Electro-Thermal Modelling of High Power Light Emitting Diodes Based on Experimental Device Characterisation

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Abstract: This paper presents a 3D finite element model for the electro-thermal analysis of high power light emitting diodes (LEDs). The proposed model and implementation approach require basic electrical and optical parameters that may be experimentally derived with the aid of advanced post-processing techniques. Extensive experimental validation reveals the capability of the model to accurately simulate self-heating, current crowding, forward voltage and other relevant performance indicators.
Keywords: Power LED, electro-thermal modelling, self-heating, current crowding.

1. Introduction

As part of the continuous efforts to boost the performance of high power light emitting diodes (LEDs), improvements in die layout and package design are broadly considered key aspects for enabling high current density operation, which constitutes a pathway towards the realisation and commercialisation of high flux emitters.

Besides the obvious trend for further reducing thermal package resistance, the increase of current density poses other significant design challenges to deal with lateral current spreading issues in the thin conducting layers of the power LED. Namely, current crowding becomes exceeding near the contact edges, thereby producing several unwanted effects that may compromise both the performance and the reliability of the device. Such effects include thermal hot spots, high non-uniform current distribution in the active layers, and increased series parasitic resistance.

In this paper, a 3D finite element (FE) electro-thermal model of InGaN/GaN flip-chip LEDs [1, 2] mounted in a high power package is presented. In such devices, the elimination of the growth substrate and wire bonds and the redistribution of the n-contact metallisation result in improved high power performance and greater versatility in attachment of optics and surface mounting [3]. Light is extracted from the substrate side as illustrated in Figure 1. Thus, the n-layer, to which the cathode is connected, and

substrate are transparent, whereas the p-contact metallisation (anode) is highly reflective. Both n- and p-layers are electrically contacted from the side of the p-layer. In order to access the n-layer, openings may be formed by etching away the p- and active layers. The n-contact electrically contacts the n-layer through these openings, which are located along the peripheral edge as well as in the inner area of the chip in the form of 16 distributed via contacts.
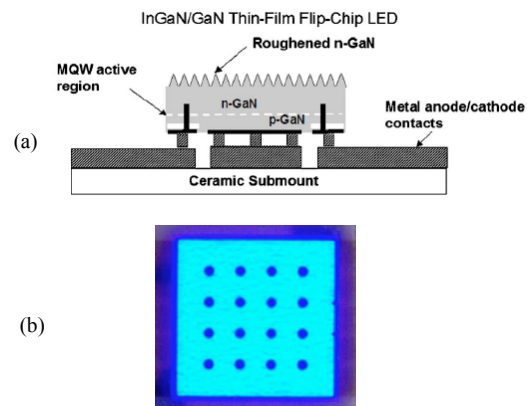

Figure 1. (a) Schematic cross-sectional representation of the InGaN/GaN thin-film flip-chip LED. Same-sided anode and cathode are shown connected with gold interconnects to a ceramic submount. (b) Plan view photo-micrograph of the device operation.

Figure 2 shows the LED package under consideration. Featuring low thermal resistance (about 9K/W), high current operation (about 1.5A) and light output capabilities (over 175lm in 6500K white), this package allows experimental investigations of the aforementioned current spreading issues.

The proposed FE modelling approach accurately predicts the quasi-static electro-thermal behaviour of the power LED in a wide range of current and temperature operation. Unlike other recent advanced FE models for current spreading analysis in LEDs [4-7], all electrical parameters of the proposed model are derived from experimental characterisation. That is, by applying the right testing conditions, individual device characteristics can be effectively measured as function of fundamental

variables, such as the junction temperature and the applied voltage. The resulting data are then fed into the model in the form of multivariable fitting functions or look-up tables. As it will be shown, the derivation of some of these characteristics may further involve advanced post-processing algorithms of system identification in order to extract the relevant information from the measured data.
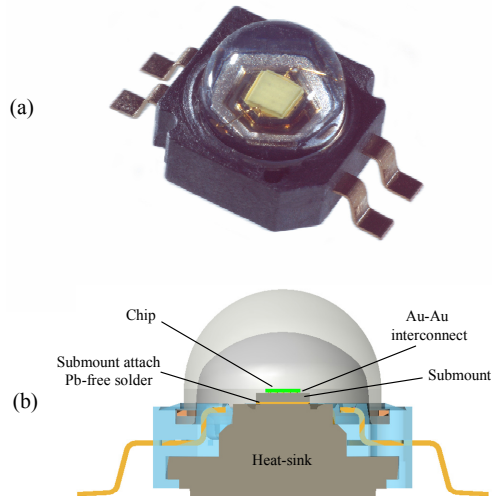

Figure 2. (a) LUXEON® K2 emitter. (b) Cross-sectional representation of a LUXEON® K2 emitter.

The independently measured electrical characteristics adequately combined with the governing equations, boundary conditions, materials' thermal conductivities and physical geometries of the chip and package structure yields fine estimations of the current density and temperature profiles across the entire die. Boundary integration calculations further provide assessment of the forward voltage, breakdown of loss contributions to heat generation and quantification of self-heating effects as function of the total current and heat-sink temperature.

The determination of these fundamental quantities sets the basis for the identification of crucial device parameters and the layout of roadmap targets and design guidelines for future device developments.

Model validation is based on extensive experimental data, where current-voltage characteristics (IV-curves) and surface brightness measurements of different die layouts are compared against simulations. Overall thermal performance predictions are also contrasted with thermal measurements.

Other relevant features of the proposed model are fast and stable numerical simulations that can be achieved despite of the inherent highly non-linear characteristics of the active region (AR) as well as the large aspect ratios of the simulated geometry. This has been possible by means of a proper FE mesh combined with adequate simplifications of the device structure.

2. Model and implementation approach

The fundamental quasi-static electric behaviour is well described with the governing Poisson's equation and Ohm's law, which are coupled with Fourier's law of heat conduction to cope with the underlying physics. Figure 3(a) shows a basic cross section of the flip-chip LED's electric stack of layers, which may be fully modelled with the FE software. However, since the AR and p-contact conductivities are dependent on the local applied voltage, the resulting model may require the use of either of the following features:

1. Definition of the AR subdomain conductivity by means of a function dependent on the local electric field
2. Use of assemblies and extrusion coupling variables to define the contact resistivity at the semiconductor p-metal interface as function of the local voltage drop
3. Use of multiple independent domain variables for the potential (e.g. $V1$, $V2$, … , Vn) that can be coupled by extrusion coupling variables so as to define the contact resistivity at the semiconductor-metal interfaces

The above advanced implementation approaches may lead to rather long simulation times and high computation power.

Fortunately, the model implementation may be dramatically simplified by assuming that lateral current spreading only occurs in the n-layer, provided that both AR and p-layer are much thinner and less conductive than the n-layer. Therefore, the model structure can be reduced to the scheme of Figure 3(b), where the AR is represented as a contact resistance boundary between the semiconductor layers.

Furthermore, given that lateral current spreading is negligible in the p-layer, both the AR and the p-contact characteristics may be combined in one single function, thereby yielding the simplified scheme of Figure 3(c).
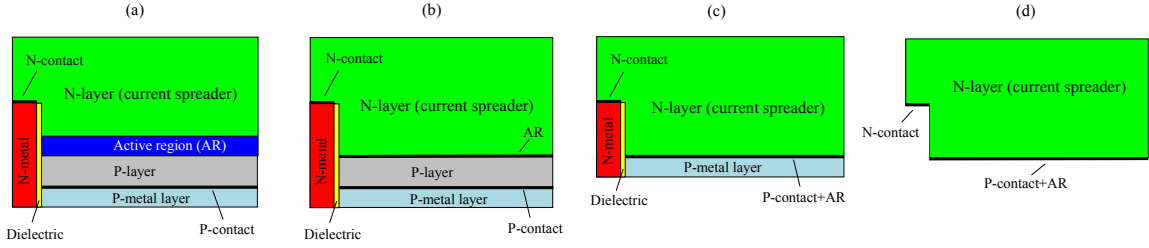
Figure 3. Basic model implementation approaches. (a) Consideration of all main layers as subdomains and use of two interior boundaries to describe the metal-semiconductor contact resistivities. (b) Elimination of the AR subdomain. AR is then defined at the interior boundary between the p-layer and the n-layer. (c) Elimination of p-layer and combination of AR and p-contact characteristics at a single interior boundary. (d) Elimination of metal layers and dielectric, thereby leaving out interior boundaries.

Finally, the elimination of the metal layers further allows avoiding the use of assemblies and/or extrusion coupling variables, and thus eventually reducing the electrical representation to a single subdomain (i.e. the n-layer) with boundary defined AR and metal-semiconductor contact resistivities, as follows,

$$n \cdot J = \frac{V}{\rho_{nc}(T)} \; , \; n \cdot J = \frac{Vf - V}{\rho_{AR\_pc}(Vf - V, T)} \quad (1, 2)$$

where ρ_{nc} is the specific n-contact resistance (typically expressed in Ω-cm^2), ρ_{AR_pc} is the combined specific AR and p-contact resistances, also expressed in the same units. Voltage Vf is the applied voltage and J is the current density. V and T are, respectively, the local voltage and temperature with respect to a reference plane.

The FE mesh arrangement is the next relevant aspect to be considered. Namely, the aspect ratio of the thin film materials to be modelled is sufficiently high to assume that the vertical component resistance (i.e. that one normal to the spreading directions, say coordinate z) is negligible. Thus, the number of elements in the z-direction can be reduced to unity without losing significant accuracy.

The proposed approach is shown to provide significantly faster and more stable numerical simulations. Accuracy is mainly determined by the ability to provide the right model parameters, which is addressed in the next section.

3. Model parameter extraction

In this section, a summary of the required parameters and associated extraction procedures is presented. An algorithm of system identification implemented with the script language is also shown to effectively allow for the determination of the AR characteristics,

which represent one of the main parameters of the model.

Table I lists the four electric parameters required by the model. Three of them, ρ_{nc}, ρ_{pc} and ρ_n may be experimentally derived from the standard transfer length method (TLM), [8-9], using circular TLM (cTLM) patterns and associated linear extrapolation methods for the parameter extraction [10].

The measurement and extraction of the specific AR resistance ρ_{AR} may involve a more sophisticated technique, for the basic contact arrangement implies lateral current spreading in the n-layer, and thus non-uniform current density through the AR. Therefore, an algorithm of system identification [11] is proposed and implemented with the script language that takes into consideration the distributed nature of the device structure in order to accurately determine ρ_{AR} from measured IV-curves. A test emitter with simplified layout (referred to as a single side n-contact emitter) is employed which allows 2D modelling representation, as shown in Figure 4. cTLM test patterns are built on wafer nearby the single side n-contact emitter so as to determine the required model parameters. The algorithm operates as illustrated in Figure 4, i.e.,

- An initial guess value for $\rho_{AR}(V,T_x)$ is determined based on the low current regime of the measured data at constant temperature T_x
- Both measured and simulated IV-curves are compared at temperature T_x. The error is then evaluated to produce a refined $\rho_{AR}(V,T_x)$
- The structure is again simulated with the new guess values
- The loop is repeated until the measured and simulated IV-curves match within a certain tolerance error. Several hundred of iterations may be required to extract the curve at one

single temperature. Thus, the use of simplified geometric test patterns (such as the proposed single side n-contact emitter) turns out to be convenient to reduce computation times

Note that for consistency with (2), the following equation must be fulfilled,

$$\rho_{AR\_pc}(V1+V2,T) = \rho_{AR}(V1,T) + \rho_{pc}(V2,T) \quad (3)$$

4. Simulation and experimental results

The electro-thermal physics must conveniently be coupled in order for the quasi-static model to provide predictions of device self-heating and associated effects on current crowding and forward voltage. Thus, simulations involve mutual dependencies where parameters of one domain (such as material properties) vary with the values of the other domain and vice versa. More explicitly, the thermal dependency in the electric model is established in all resistive parameters, as already indicated in Table I. On the other hand, the heat source represents the parameter from the thermal model that depends on an electrical quantity. Such quantity corresponds to the portion of the consumed electric energy that is not converted into photons and thus it produces heat. The amount of generated heat can be obtained by computing the total power density and subtracting from it the contribution to light generation, which is determined by the wall-plug efficiency (WPE). The WPE may by itself be current density and temperature dependent. By means of 2D look up tables and proper interpolation functions, the model employs experimental WPE data containing such dependencies.

TABLE I: Summary of model's electric parameters and characterisation techniques for their determination.

| Parameter	Units	Variable of dependence	Measurement technique	Test structure	Extraction method
Specific n-contact resistance ρ_{nc}	Ω-cm^2	T	TLM	cTLM	cTLM equation, linear extrapolation
Specific p-contact resistance ρ_{pc}	Ω-cm^2	V, T	TLM	cTLM	cTLM equation, linear extrapolation
N-layer resistivity ρ_n	Ω-cm	T	TLM	cTLM	cTLM equation, linear extrapolation
Specific active region resistance ρ_{AR}	Ω-cm^2	V, T	IV curve tracer	Single side n-contact emitter	Algorithm of system identification
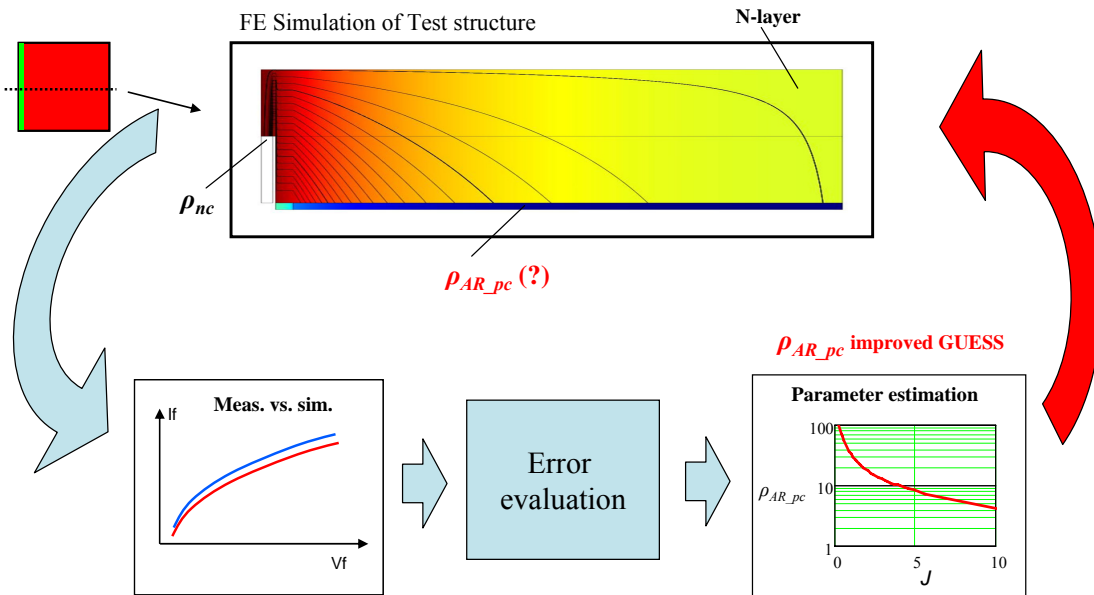
Figure 4. Principle of operation of the proposed algorithm of system identification for parameter extraction.

The generated heat is assumed to be entirely transferred from the chip to the heat-sink via the interconnect layers. Figure 5(a) depicts the heat flux at the interface between the epitaxial layer and the first deposited layers of metal and dielectric. In this illustration, the regions of high heat flux correspond to those of current crowding, namely, the corner and via edges.

Figure 5(b) illustrates simulation results of the thermal distribution across the chip surface. Temperature is referenced to the heat-sink base (Tcase). Simulation reveals hot spot areas in the edge of the chip, particularly in the corners. The coolest areas of the chip coincide with the regions of metal interconnection to the substrate (see Figure 1(a)). Estimation of the thermal resistance based on the average temperature rise and dissipated power matches up closely with experiments, i.e. 9.6K/W.

Extensive validation of the electrical model and characterisation procedures described in the previous section has been carried out by comparing simulated and measured IV-curves of different die layouts at constant temperature (i.e. measurements under pulse conditions). This is shown in the plots of Figure 6. Up to four different primary designs have been tested that highlight the model ability to accurately predict the variations in the electrical response caused by changes in the layout geometry. The layouts considered are four: (1) ring LED with inner and outer edge n-contact, (2) square LED with a single centre n-contact via and no edge contact, (3) square LED with edge n-contact and no centre vias, and (4) square LED with one single n-contact side. The simplicity of the layout further allows fundamental investigations of current distribution in thin film layers. Note that the measured devices correspond to wafer near neighbours, and thus the difference in the IV-curves are mainly attributed to layout geometry.

In addition, surface brightness measurements are performed as an approach to experimentally estimate the current density profiles of the different LEDs under test. The existing correlation between the measured irradiance and the current density allows converting the simulated current density profiles into irradiance maps, and hence direct comparisons with surface brightness images can be obtained. The relation between the captured irradiance and the current density may be experimentally derived by means

of dedicated emitters featuring exceptionally low resistive spreading layers. The current flow in such LEDs is assumed to be fairly uniform.

Once the relation between irradiance and current density is introduced into the software, the surface brightness images can be estimated as illustrated in Figure 7. As it can be shown, the model predicts the strong surface non-uniformities of the different primary geometries at various current levels.

Lastly, experimental IV-curves of commercial emitters are compared to simulations. Accurate predictions without self-heating (i.e. pulse measurements) over a wide current range are shown in Figure 8. By properly monitoring the case temperature, good estimations under dc operation can also be obtained as shown in Figure 9.
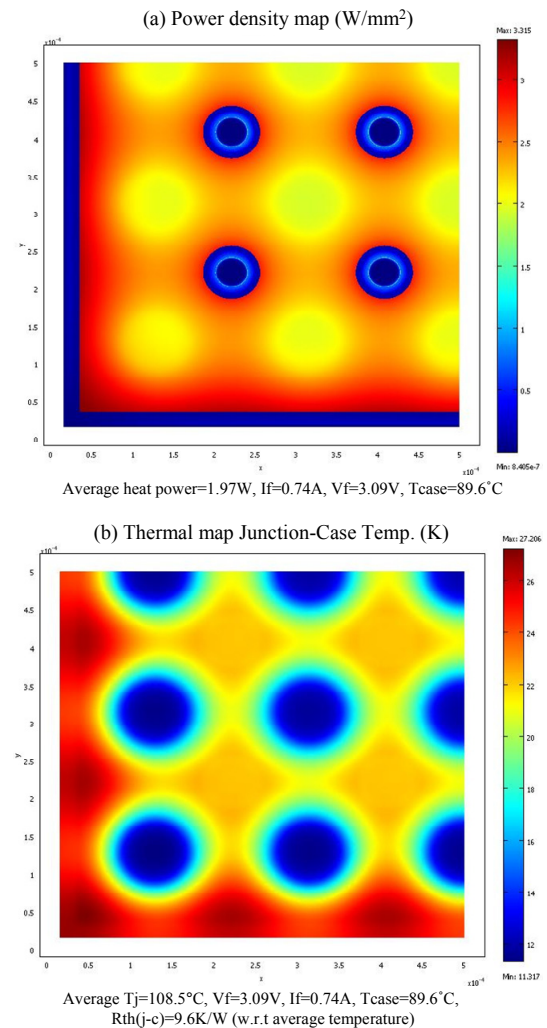

(a) Power density map (W/mm^2)

Average heat power=1.97W, If=0.74A, Vf=3.09V, Tcase=89.6˚C

(b) Thermal map Junction-Case Temp. (K)

Average Tj=108.5°C, Vf=3.09V, If=0.74A, Tcase=89.6˚C,
Rth(j-c)=9.6K/W (w.r.t average temperature)

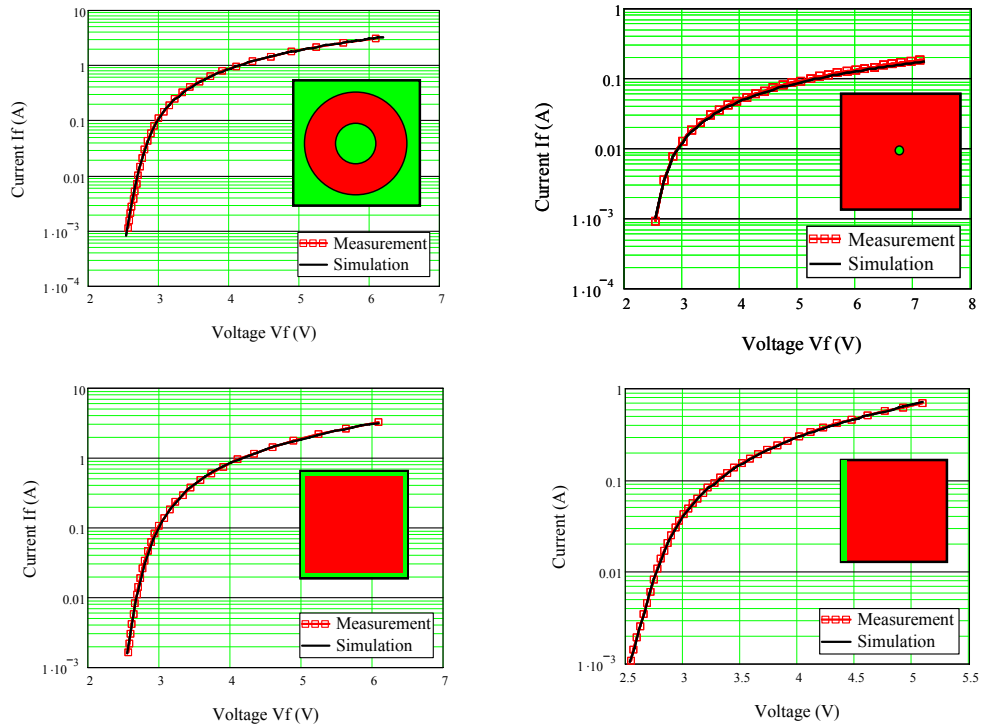**Figure 5.** Electro-thermal simulation example.

Figure 6. Experimental and simulated IV curves of various LEDs with simplified die layouts mounted on LUXEON® K2 package and operating at 30˚C (pulse conditions). Note from the die layout top views that green areas represent n-contact, whereas red areas represent active region and p-contact.
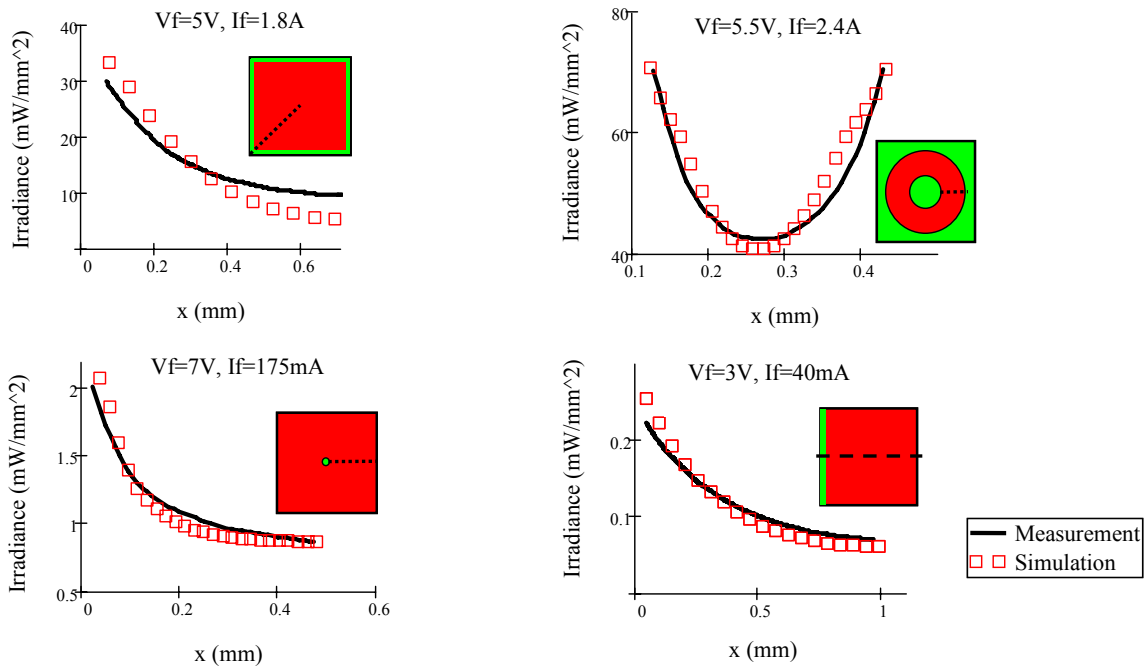

Figure 7. Experimental and simulated surface brightness of various LEDs with simplified die layouts mounted on LUXEON® K2 package and operating at 30˚C (pulse conditions). Note from the die layout top views that green areas represent n-contact and red areas active region and p-contact.
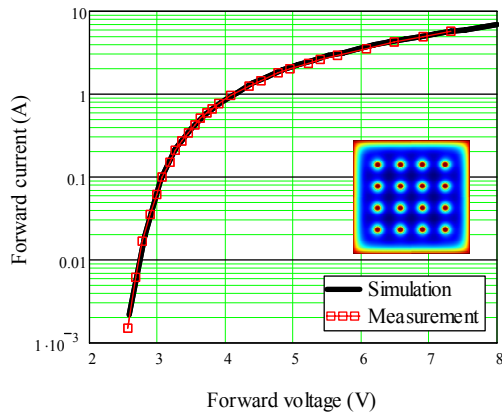
Figure 8. Experimental and simulated IV-curves of a LUXEON® K2 emitter at 90˚C case temperature.
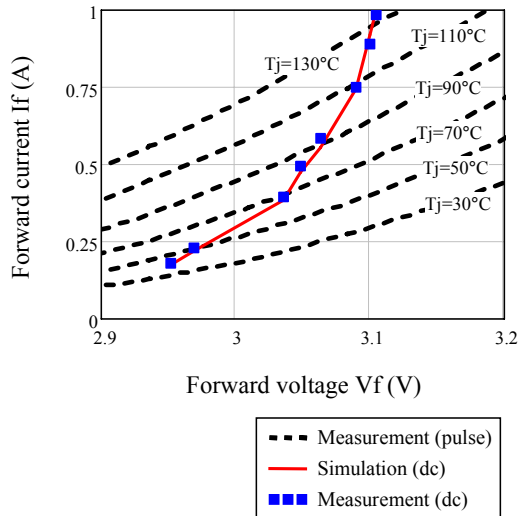

Figure 9. Experimental and simulated IV-curves with and without self-heating of a LUXEON® K2 emitter.

5. Summary and conclusions

A 3D FE model has been presented as a tool to analyse the electro-thermal behaviour of power LEDs. Current crowding, forward voltage and thermal stress have been accurately modelled over a wide range of operating conditions and for various die layouts. Thermal resistance has been predicted by providing relevant device geometry data, material parameters and optical performance. Experimental validation shows that electro-thermal coupled effects such as self-heating are well described and quantified.

The modelling approach describes the quasi-static electrical behaviour by means of four basic resistive parameters, all of which can be determined by experimental characterisation.

While most of the parameters may be obtained by standard techniques, the measurement and extraction of the AR characteristics critically involves the compensation of non-linear current distributed effects through the chip area and thus may require advanced characterisation techniques. An algorithm of system identification has been proposed and implemented in the script language that effectively allows determining the AR IV-curves in emitters with simplified layout geometry.

The electrical model implementation has been greatly simplified to a single subdomain, thereby resulting into fast, stable and yet accurate simulations.

6. Acknowledgements

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