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sense and simplicity

Electro-Thermal Modelling of High Power Light Emitting Diodes Based on Experimental Device Characterisation

Toni López
Comsol Conference, Boston 2008

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Outline

- Introduction
  - LUXEON® K2 Emitter
- LED Characterisation and Modelling
  - Electric model
  - Thermal model
  - Coupled electro-thermal model
- Experimental validation
- Summary

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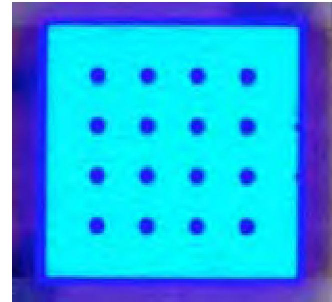
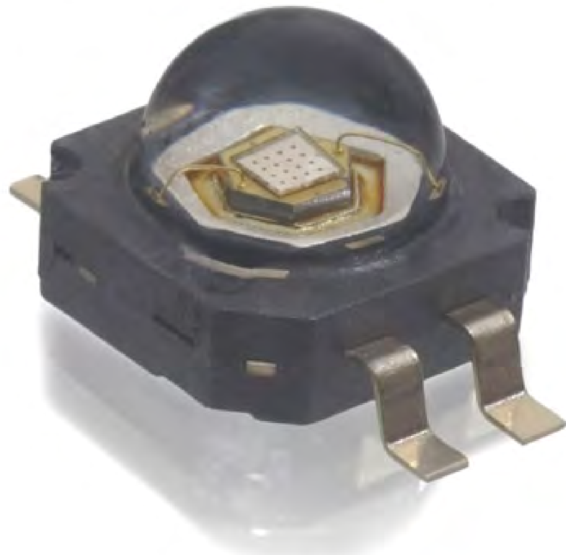
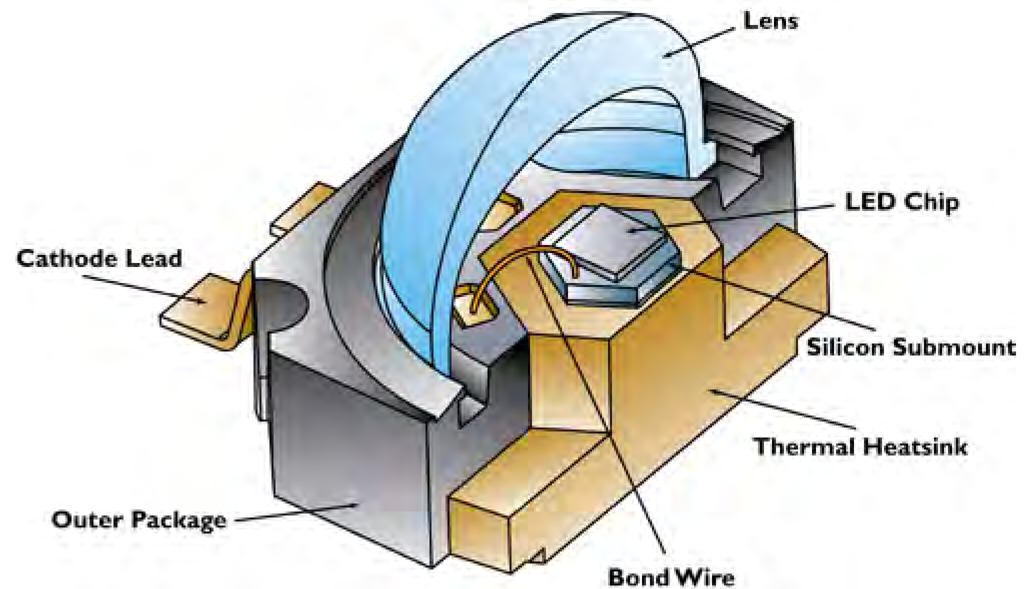
LUXEON® K2 Lamps



- The goal is to accurately model the electro-thermal performance of high power LEDs for the assessment of relevant effects such as,
  - Current crowding
  - Thermal hot spots
  - Self-heating
  - Forward voltage





Operating Specs: 1A forward current, over 200lm, 185°C junction temperature

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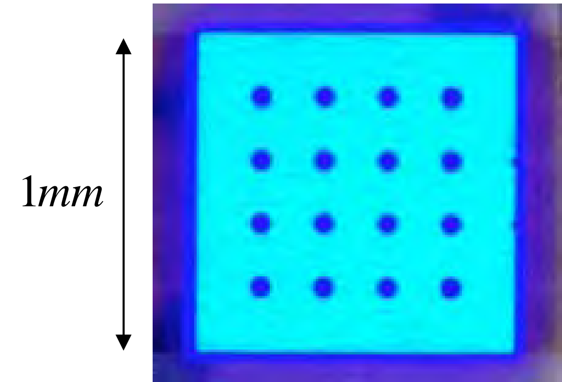
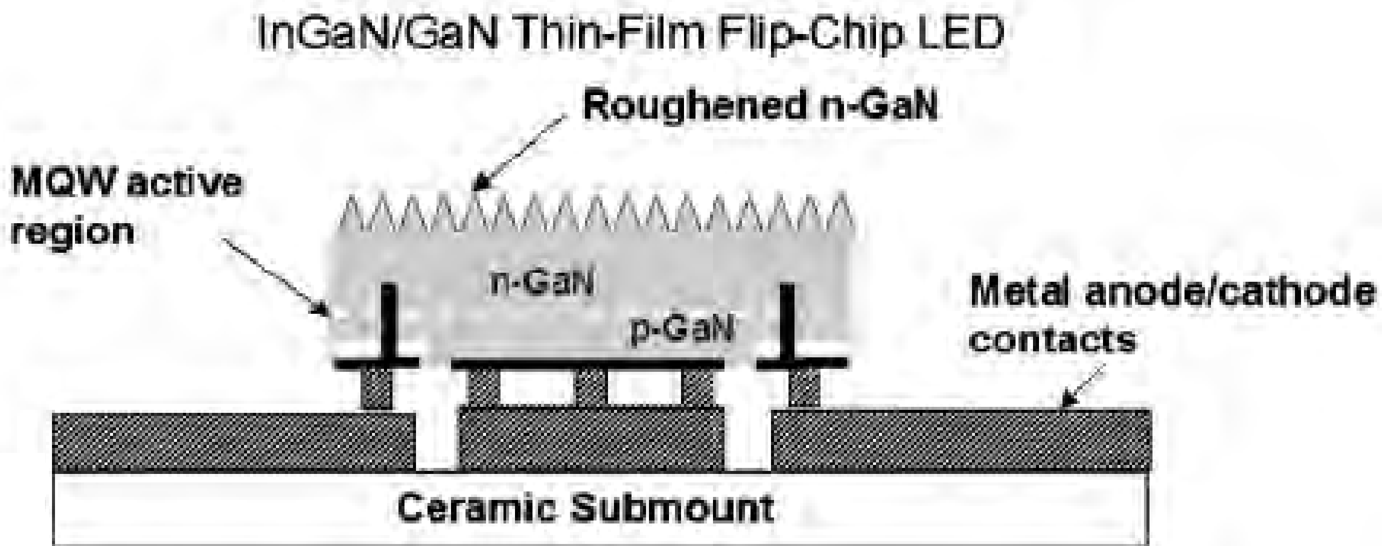
Structure of TFFC LED



- Thin-Film Flip-Chip Technology
- N-layer contacted from p-layer side by means of 16 circular vias and edge contact
- P-metal contact also acts as optical reflector
- 25 gold stud-bumps employed to interconnect chip and submount



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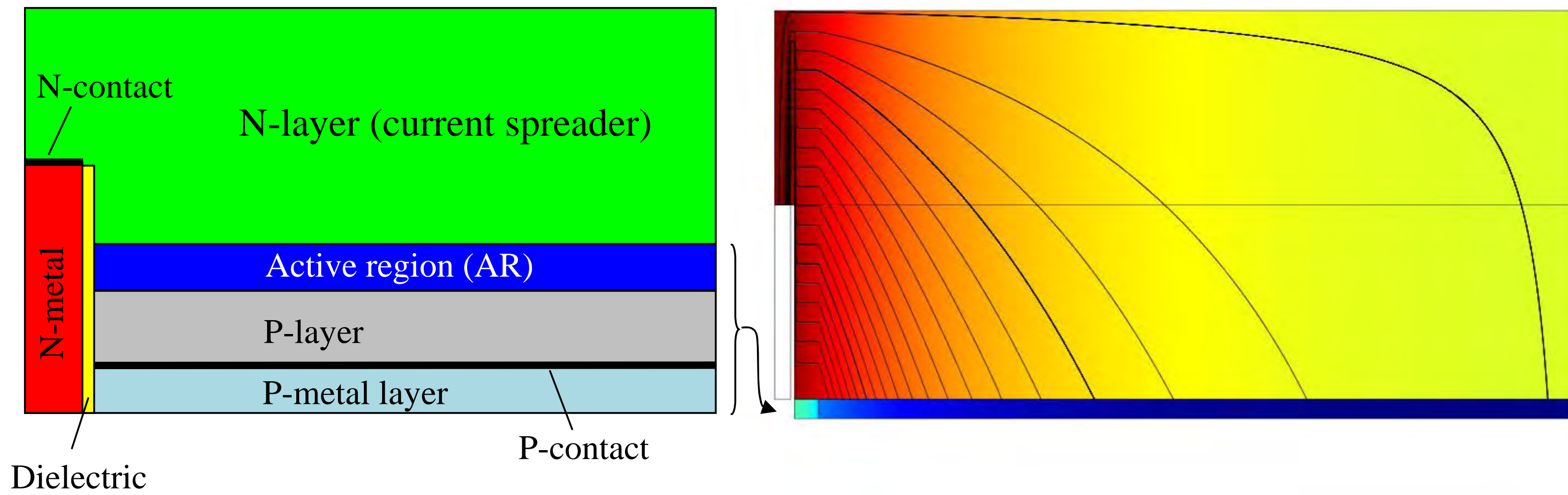
Basic Representation of the Chip Multilayer Stack

- LED chip consists out of multiple semiconductor, dielectric and metal layers, which are arranged according to the TFFC arquitecture
- Basically, the n-semiconductor sheet (of just a few microns thick) is used as spreading layer. It is the only semiconductor layer where current may flow laterally
- Thus, the distributed effects may be represented by a ladder network of lumped elements, the vertical elements being non-linear according to a diode like function and a series resistance



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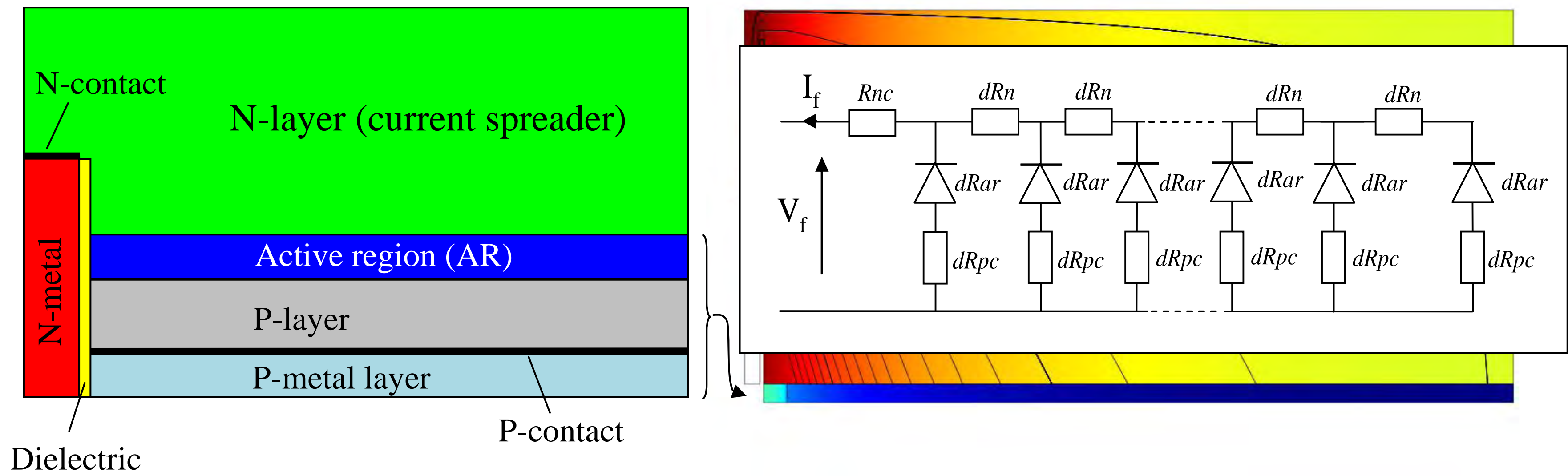

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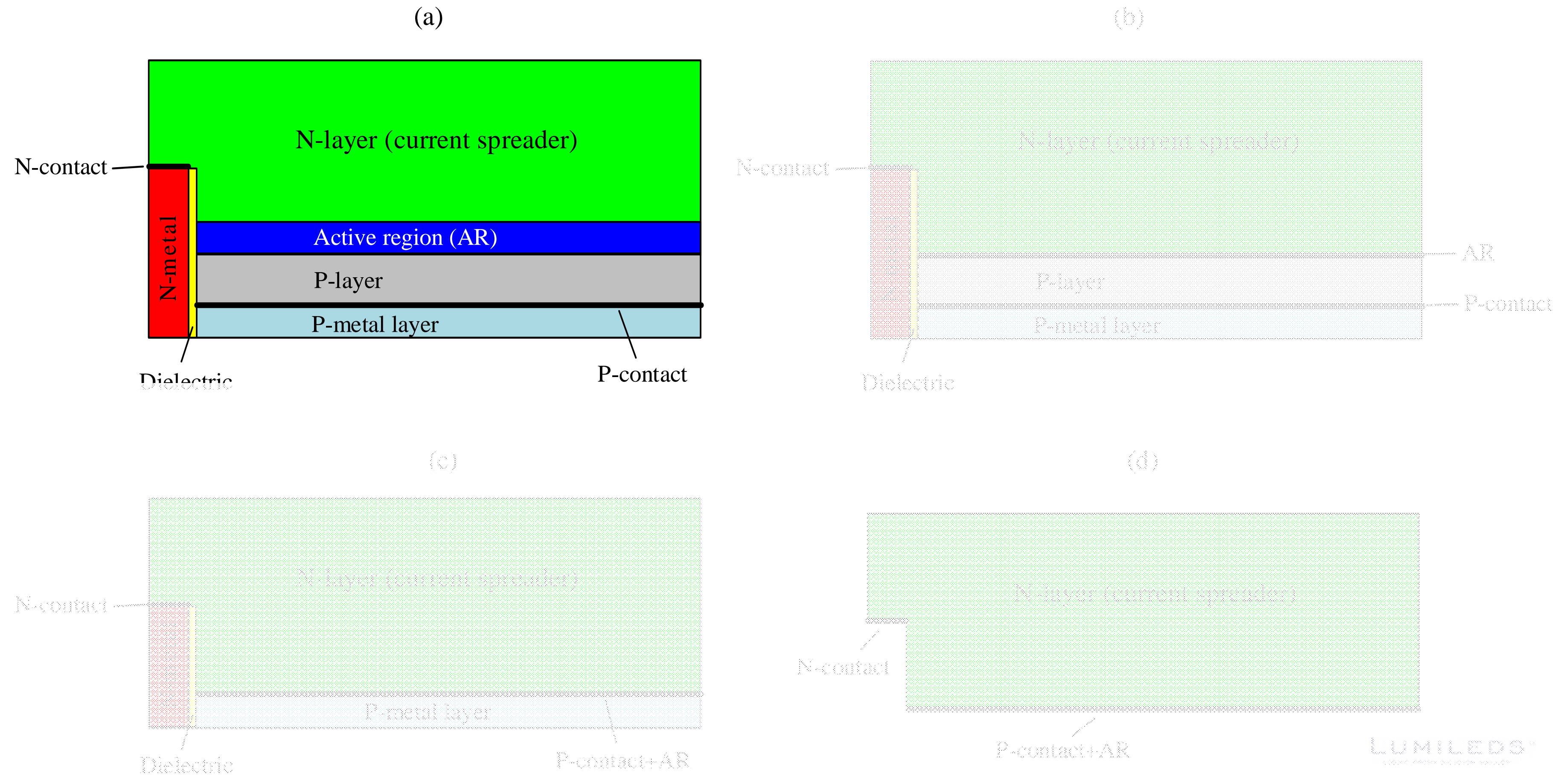
Electric Model Implementation

a) The basic multilayer stack may require up to six different subdomains. At least one of them, the AR subdomain, may involve the definition of a non-linear conductivity that is dependent on the local electric field



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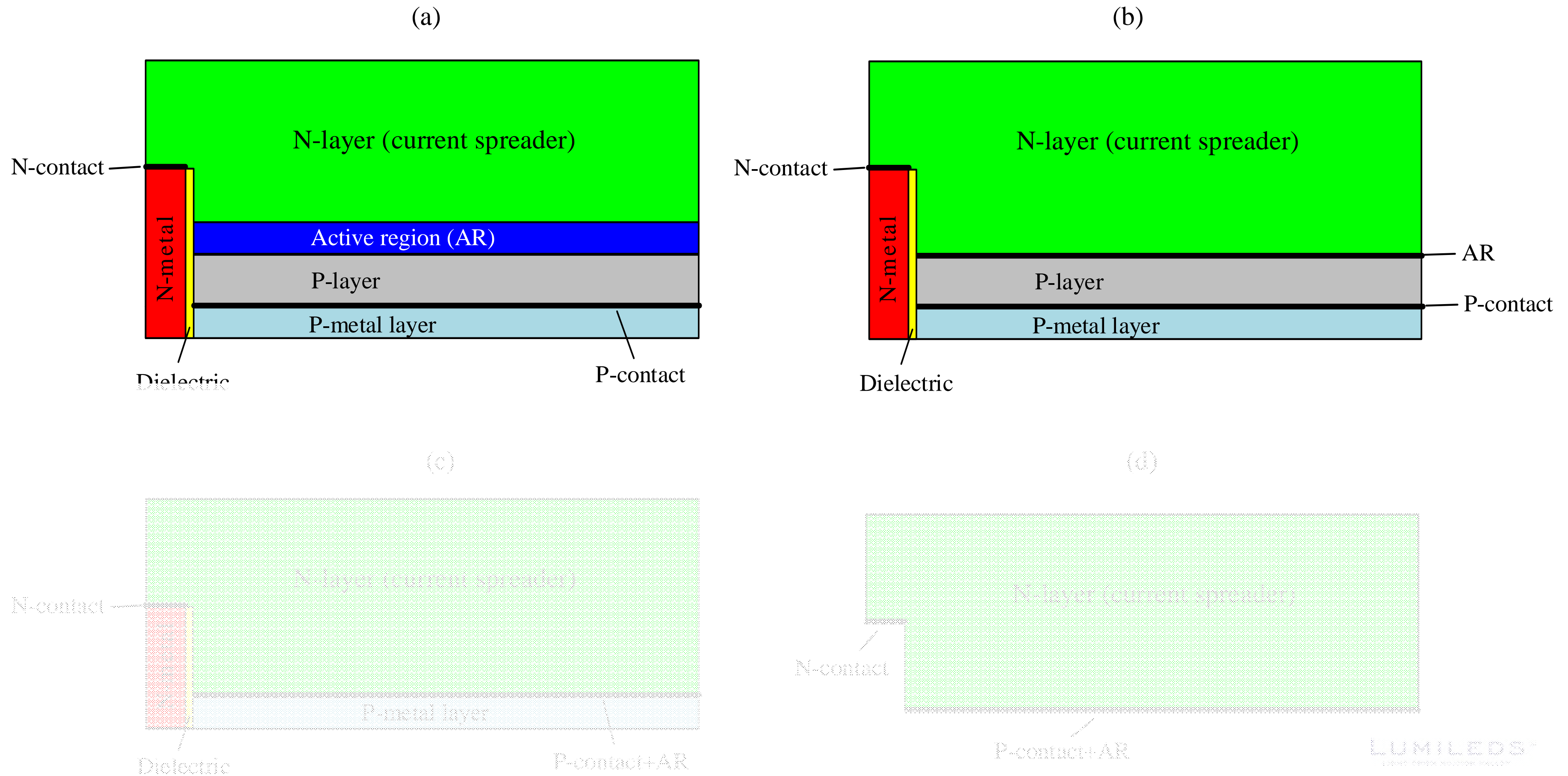
Electric Model Implementation

b) The current flows unidirectionally vertically in the AR. Thus, it may be described by way of an interior boundary condition as opposed to a subdomain. The boundary condition is of the type *distributed resistance* where the conductivity may be non-linear and dependent on the local voltage difference between the two sem. layers



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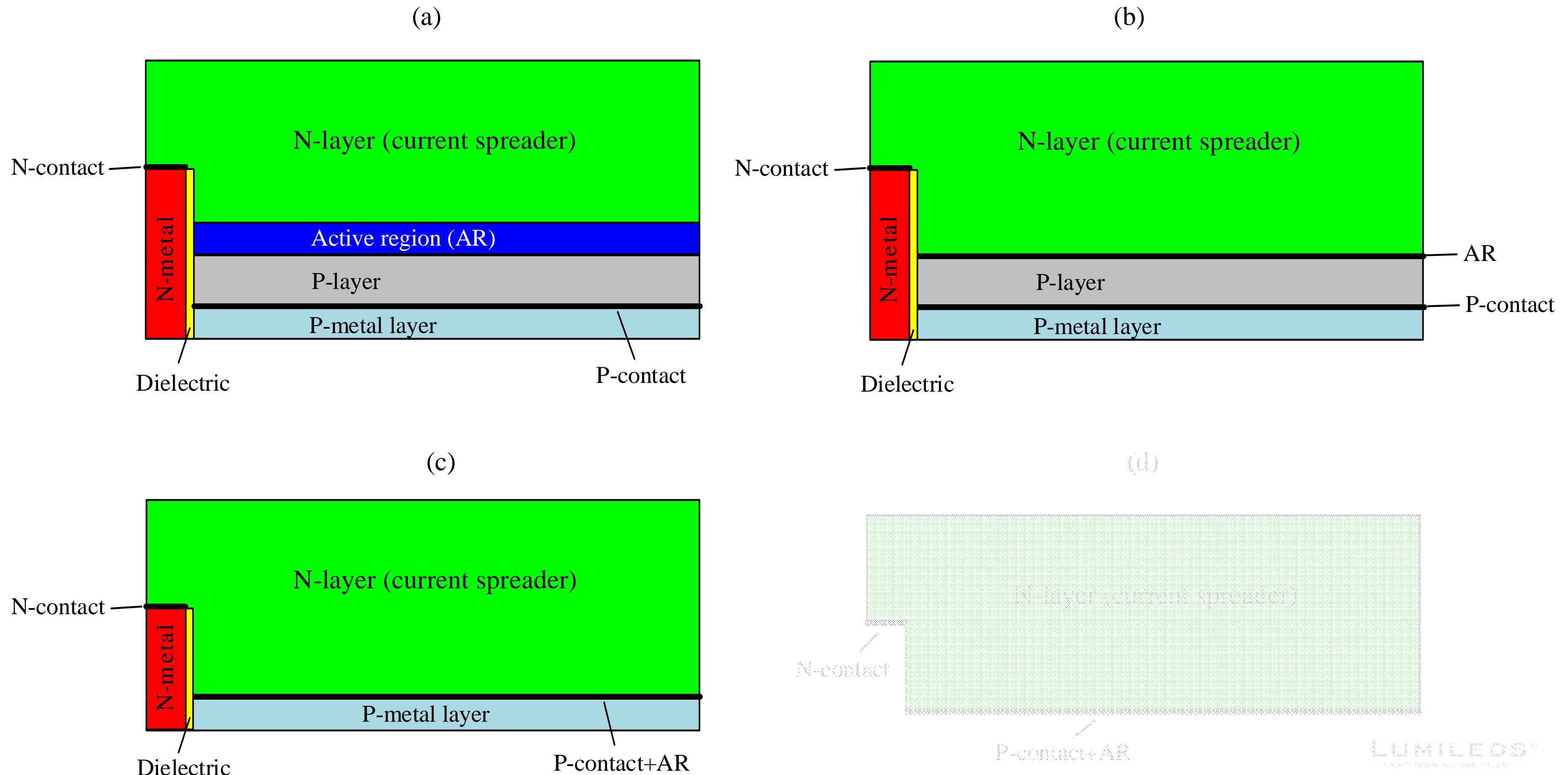
Electric Model Implementation

c) The current through the p-layer flows vertically. This layer is very thin and thus it can be omitted since its contribution to electric losses is negligible. The elimination of the p-layer involves the combination of the AR and p-contact in one single interior boundary



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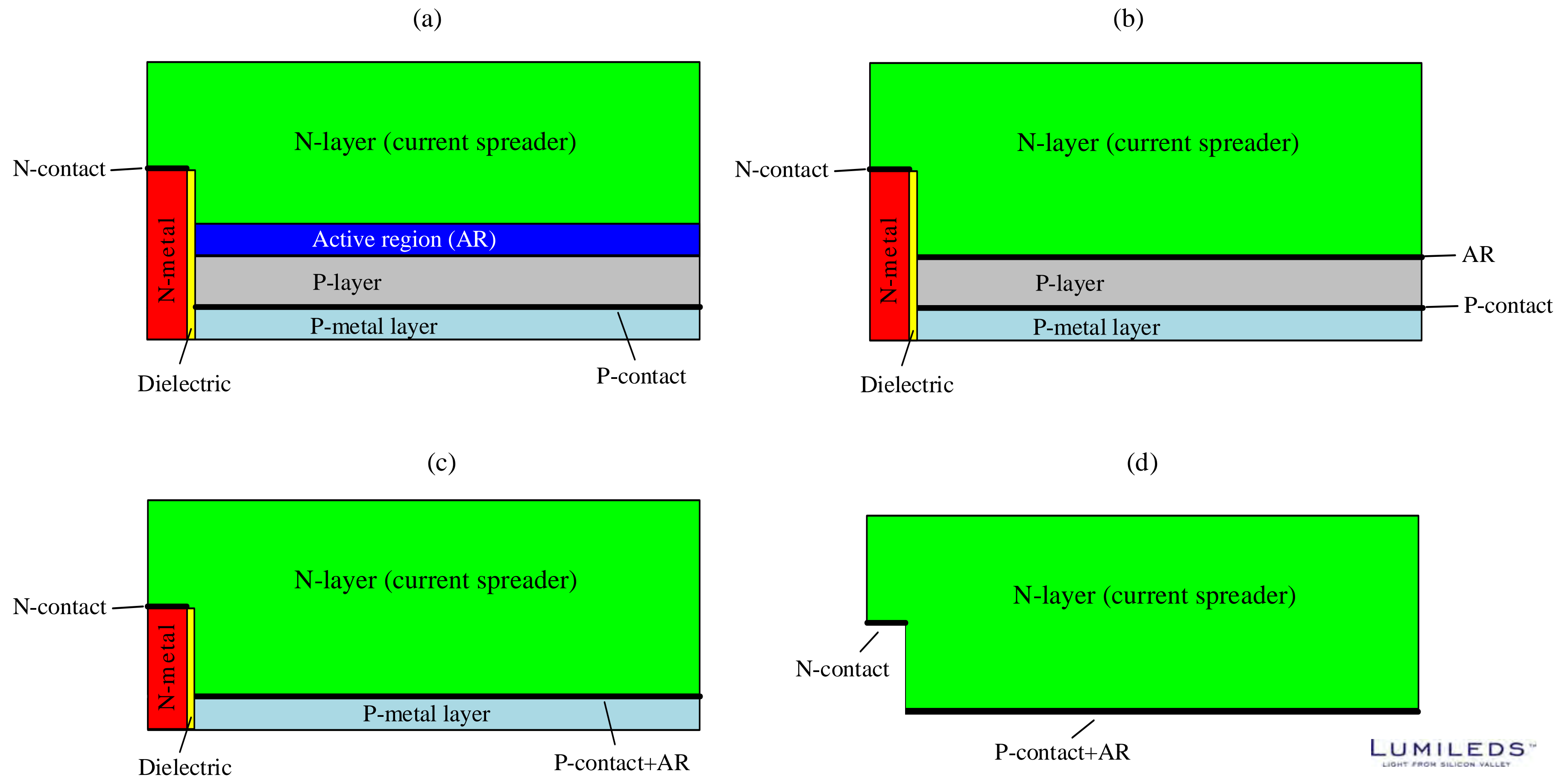
Electric Model Implementation

d) The elimination of the metal layers, which do not contribute to losses, enables the use of external boundary conditions as opposed to interior ones for the definition of the contacts and AR, thereby greatly simplifiyng the implementation



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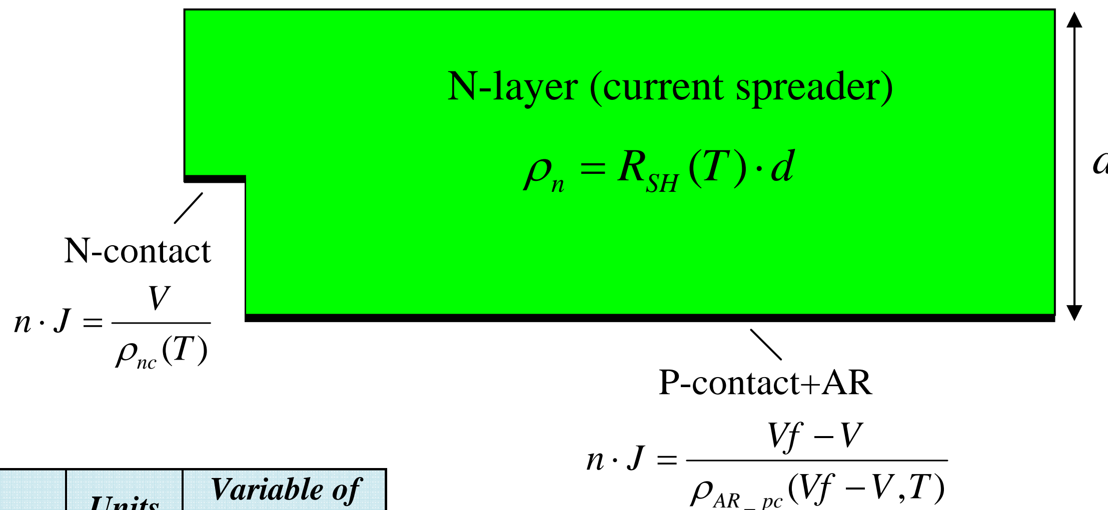
Simplified Electric Model Implementation

- Single subdomain characterised by a temperature dependent conductivity, which is described by a look up table (LUT)
- Distributed resistance boundary conditions for metal-semicond. contacts and active region (AR) representation. Conductivities may be voltage and temperature dependent. Use of LUTs



$$n \cdot J = \frac{Vf - V}{\rho_{AR_pc}(Vf - V, T)}$$

Parameter	Units	Variable of dependence
Specific n-contact resistance ρ_{nc}	Ω-cm^2	T
Specific p-contact resistance ρ_{pc}	Ω-cm^2	V, T
N-layer resistivity ρ_n	Ω-cm	T
Specific active region resistance ρ_{AR}	Ω-cm^2	V, T

$$\rho_{AR_pc}(V1+V2,T) = \rho_{AR}(V1,T) + \rho_{pc}(V2,T)$$

$R_{SH}(T)$: Sheet resistance (Ω/□). Measurable quantity

Vf : Applied voltage

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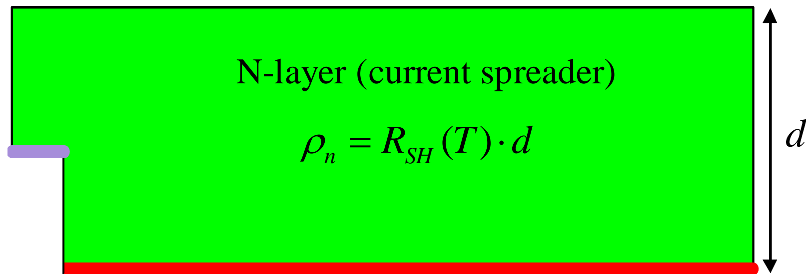
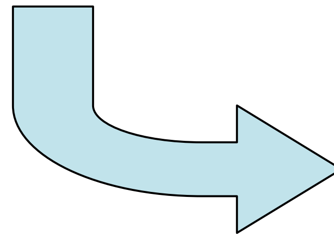
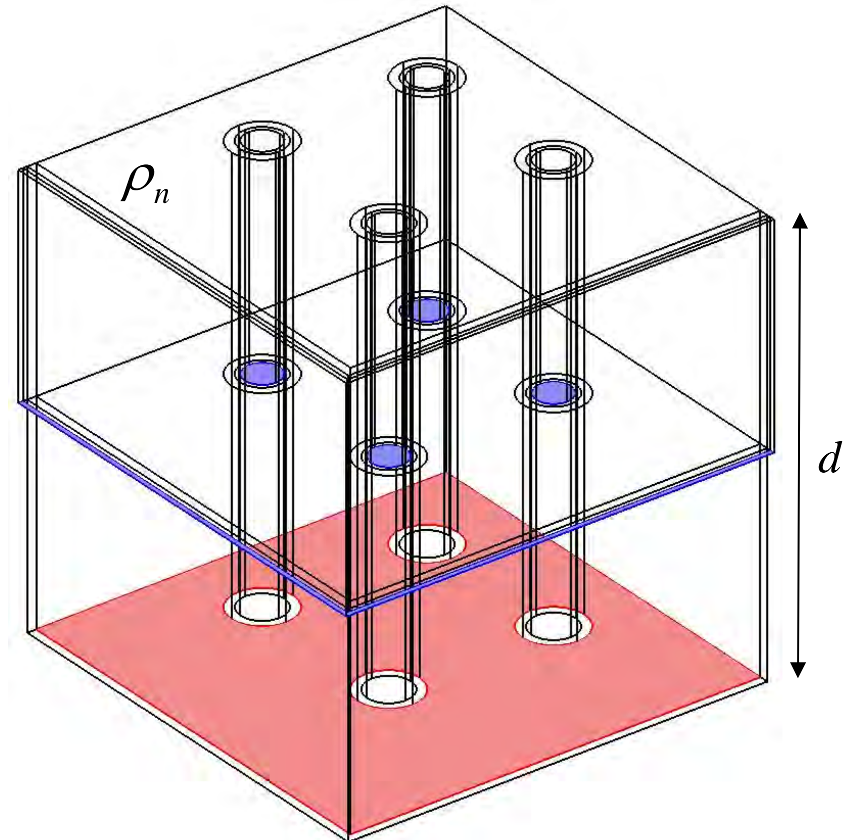
Extension to a 3D Subdomain

Simplified 2D structure





TFFC 3D structure (¼ chip)



Non-isolated boundary conditions
(Distributed resistance):

P-contact+AR	N-contact
$n \cdot J = \dfrac{Vf - V}{\rho_{AR_pc}(Vf - V, T)}$	$n \cdot J = \dfrac{V}{\rho_{nc}(T)}$

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Extraction of Device Characteristics

Parameter (No thermal params. included)	Variable of dependence	Measurement technique	Test structure	Extraction method
1. Specific n-contact resistance **2. Sheet resistance**	Temperature	TLM	cTLM	cTLM equation, linear extrapolation
3. Specific p-contact resistance	Temperature and current density	TLM	cTLM	cTLM equation, linear extrapolation
4. Active region IV curve	Temperature and current density	IV-curve tracer	Single side n-contact emitter	Algorithm of system identification
5. Radiant emittance and/or irradiance	Temperature and current density	Integrating sphere, gonometer	Single side n-contact emitter	Algorithm of system identification

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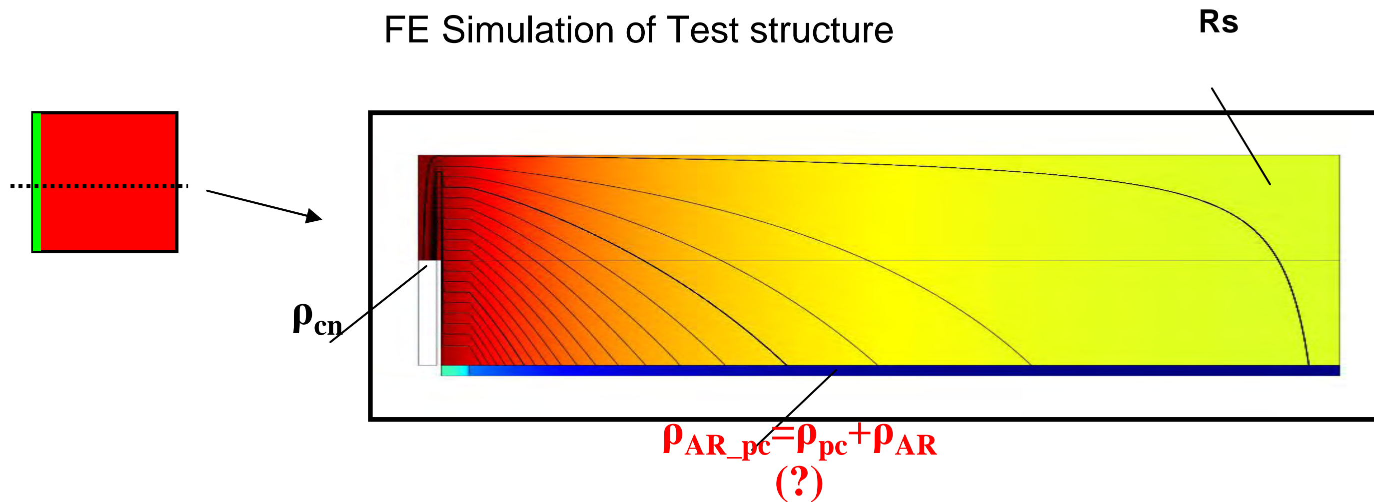
AR & P-contact resistivity extraction algorithm



- Goal: Extraction of the AR & p-contact resistivities from the IV curves measured at the device terminals
- Challenge: This is not readily obtained due to the non-linearity of the resistivities and the distributed nature of the device structure (i.e. non-uniform current distribution)
- Solution: System identification techniques. I.e. advance algorithms to determine model parameters from measured data.

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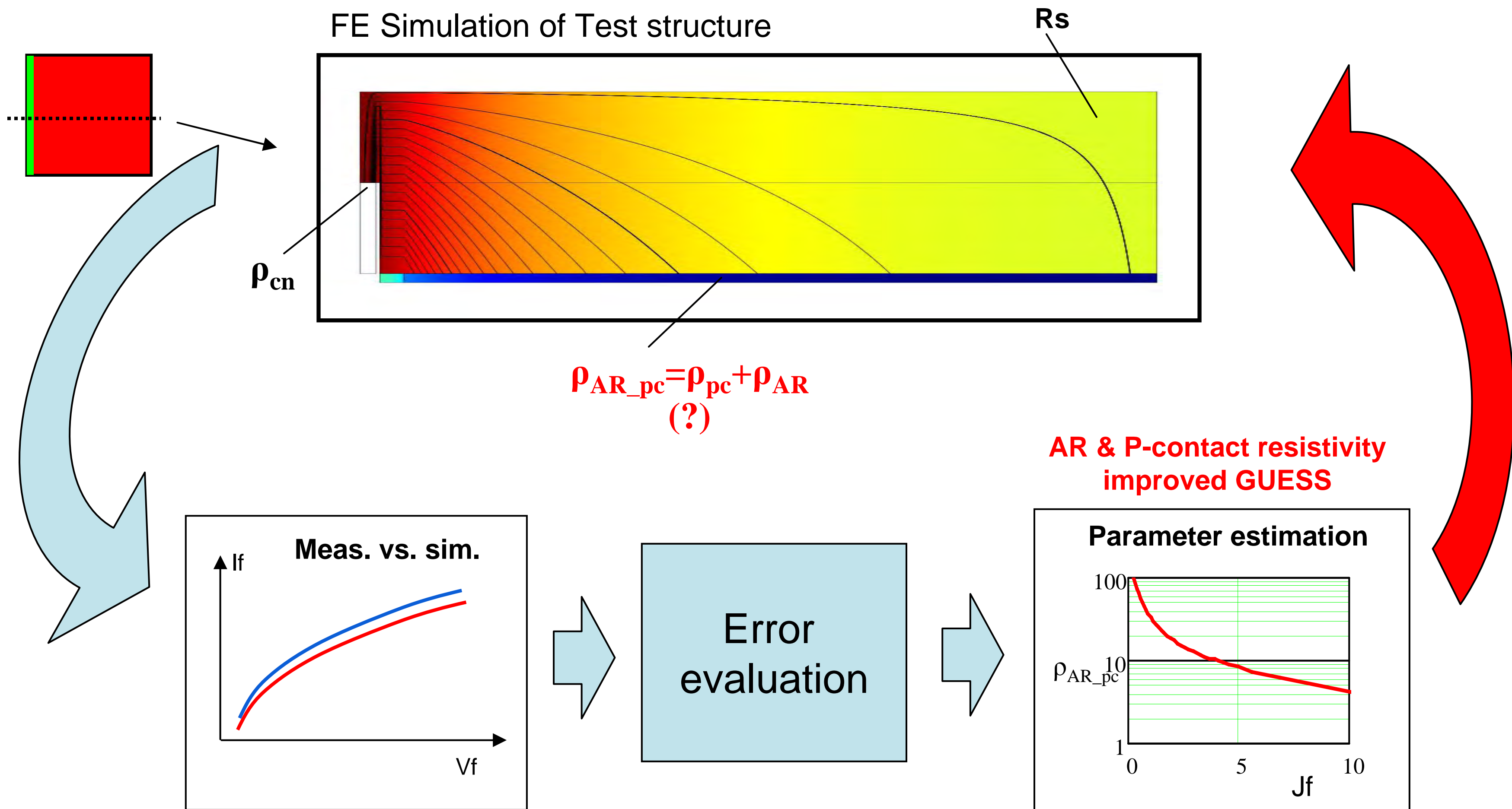
AR & P-contact resistivity extraction algorithm



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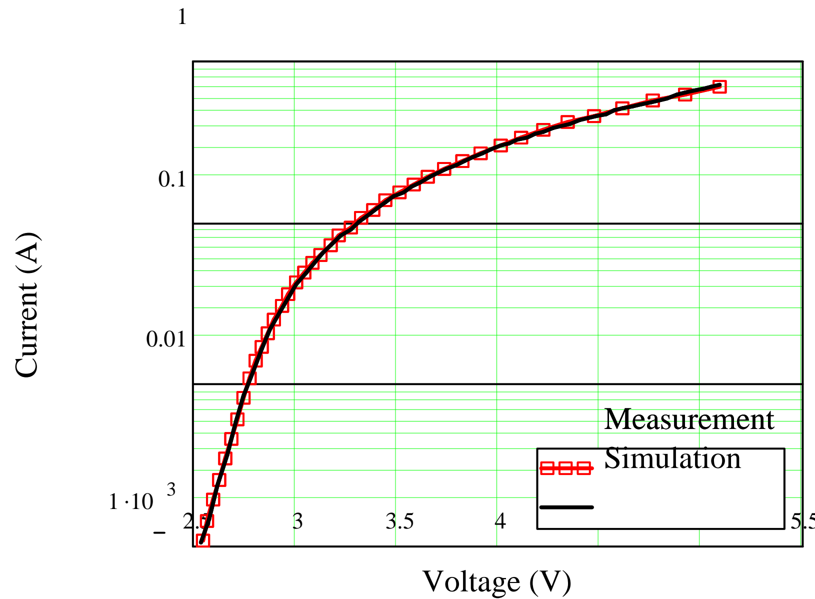
AR & P-contact resistivity extraction algorithm

FE Simulation of Test structure

Rs

Repeat loop until error is minimised



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- Goal: E … curves measured … t the i…
- Cha … of the resistivities … and … orm current … dist…
- Solu … ification techniques. I.e. advance algorithms to determine model parameters from measured data.

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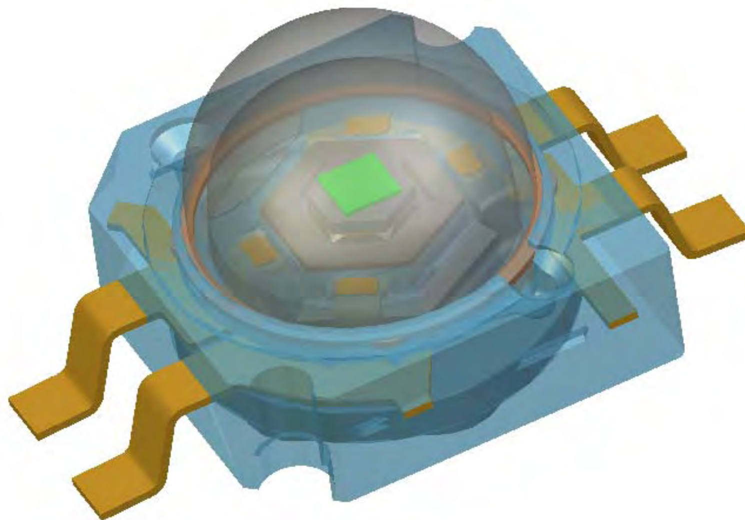
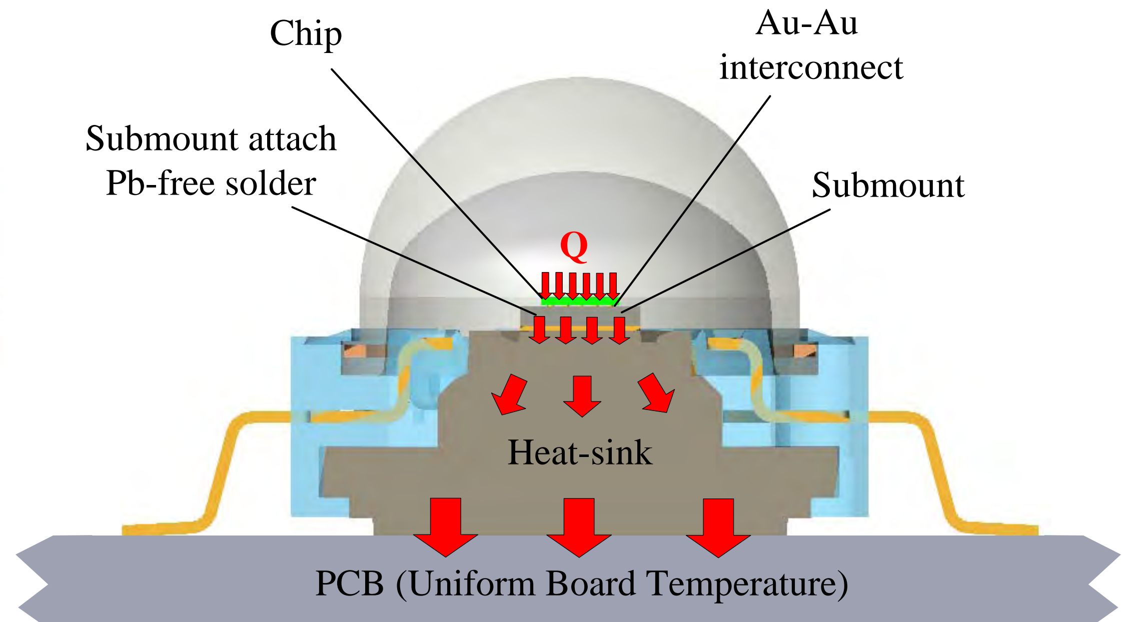
Thermal Model

- Governing equation: Fourier’s law of heat conduction
- Generated heat in the chip is transferred to the PCB through the package submount and heat-sink
- Constant board temperature (boundary condition)
- Model considers 3D package and chip geometry and all material‘s thermal conductivities





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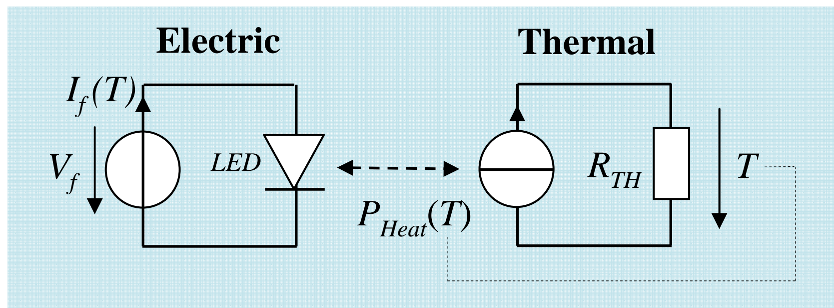
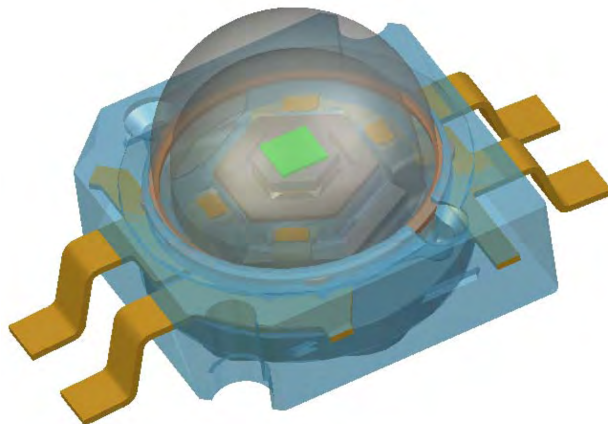
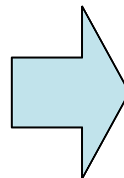
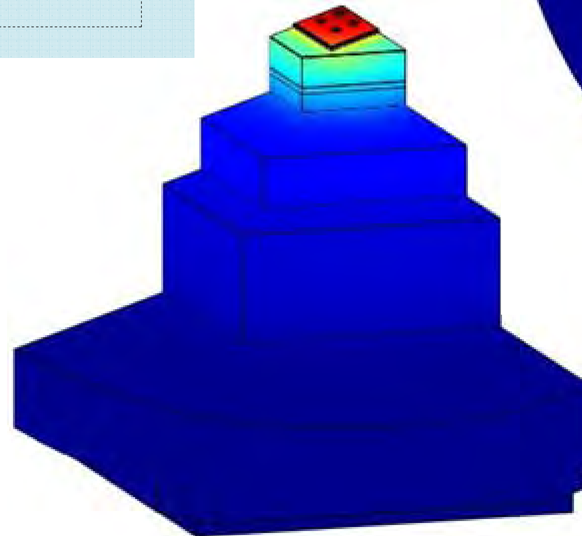
Coupling Thermal and Electric Models

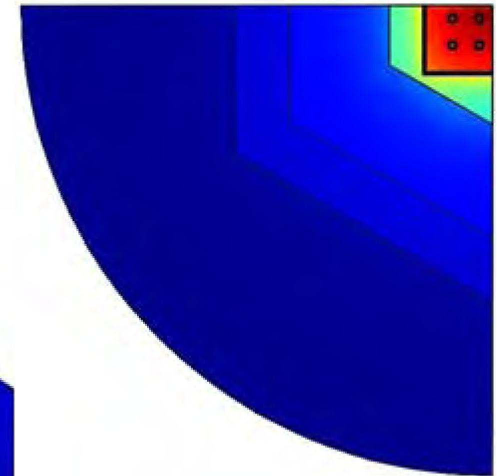
- Electric and thermal models are coupled by the mutual dependencies of the following parameters
  - Electric conductivities (contacts, spreading layer...)
  - Power dissipation: $P_{Heat}(T) = P_{Total}(T)\left(1 - WPE(T)\right)$, $P_{Total}(T) = I_f(T) \cdot V_f$











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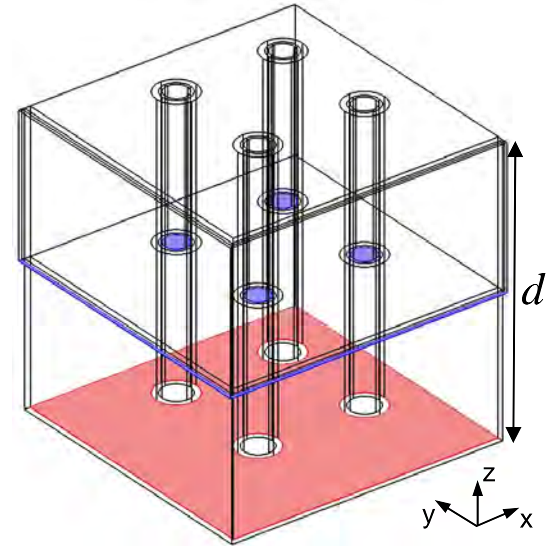
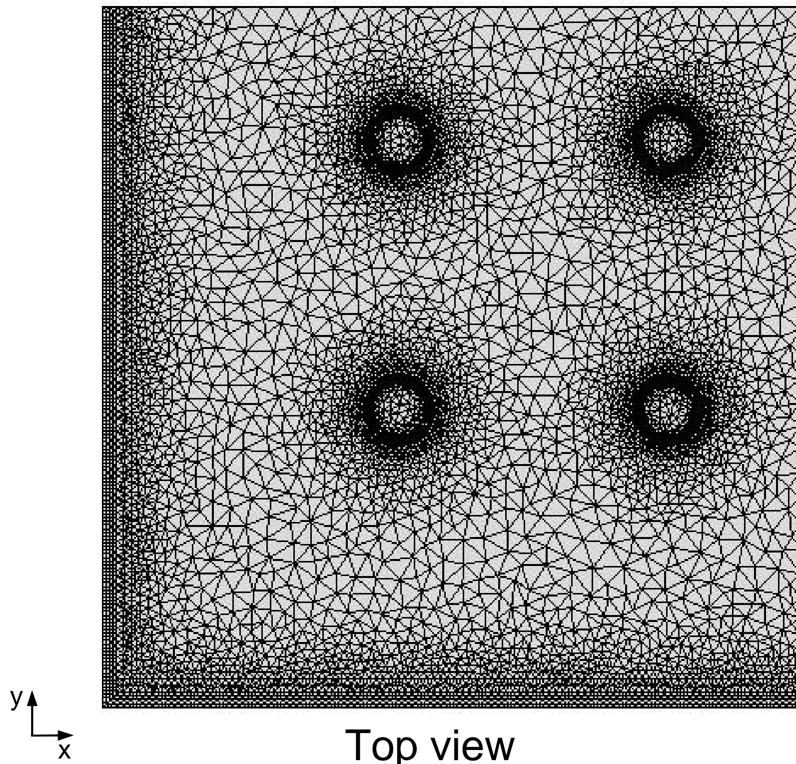
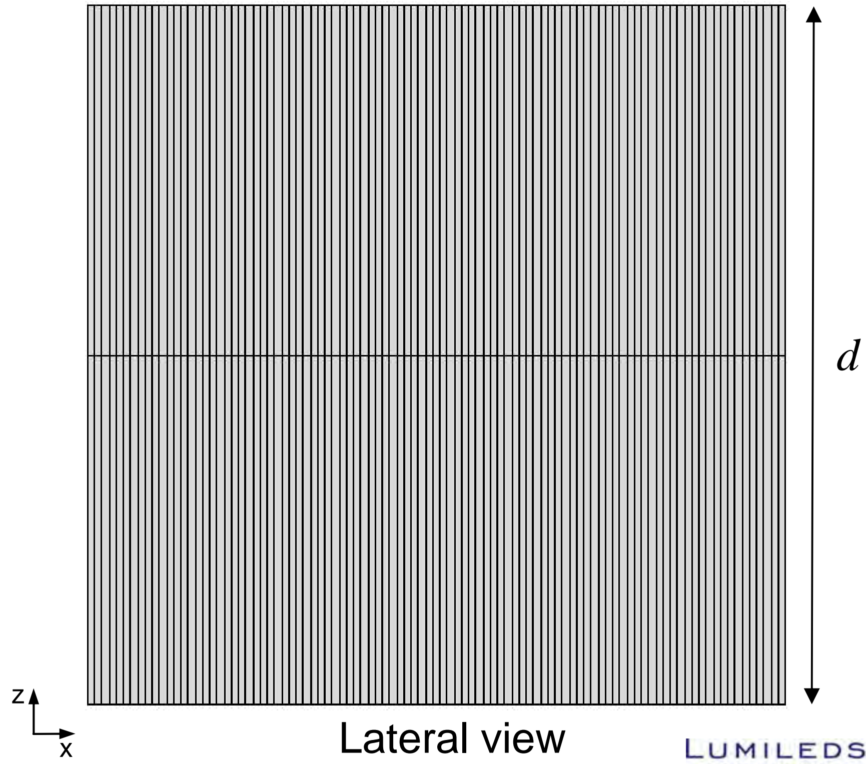
Meshing Thin Layers

1. Boundary free mesh parameters for x-y boundary plane
2. Swept mesh parameters for z (use of 2 element layers)





Top view



Lateral view

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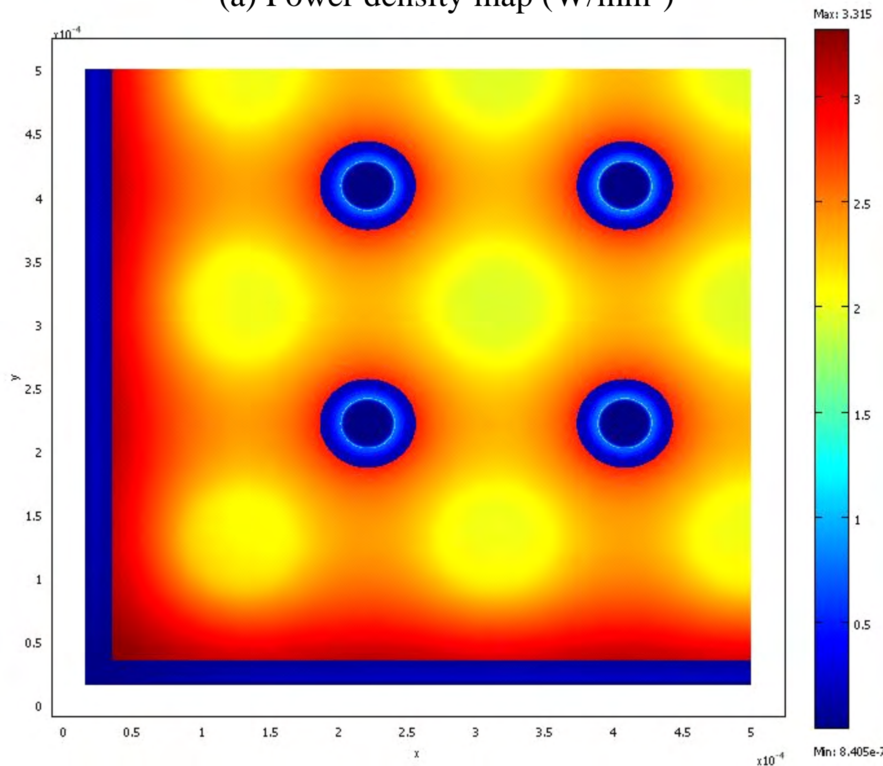
Coupled Electro-Thermal Simulation Example

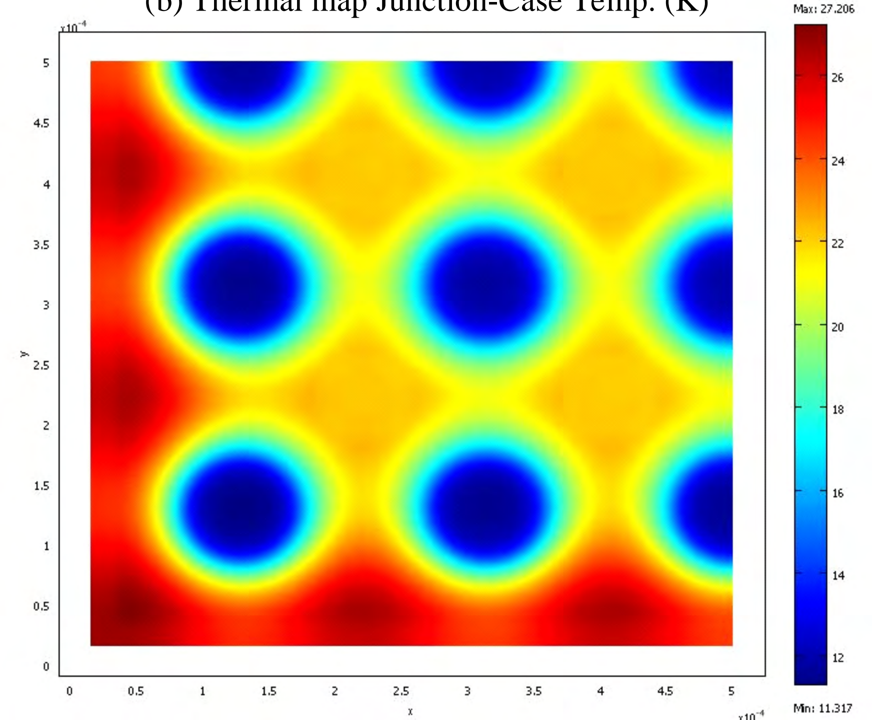
- ***Use of Direct solver PARDISO, num. mesh elements: 200600, degrees of freedom: 432429, computation time: 17min., WinXP 64bit, Intel Xeon CPU, 2.66GHz, 12GB RAM***
- Thermal non-uniformity impacts power density distribution and thus the surface brightness
- Estimated thermal resistance matches experimental results

(a) Power density map (W/mm^2)



Average heat power=1.97W, If=0.74A, Vf=3.09V, Tcase=89.6℃

(b) Thermal map Junction-Case Temp. (K)



Average Tj=108.5℃, Vf=3.09V, If=0.74A, Tcase=89.6℃,
Rth(j-c)=9.6K/W (w.r.t average temperature)

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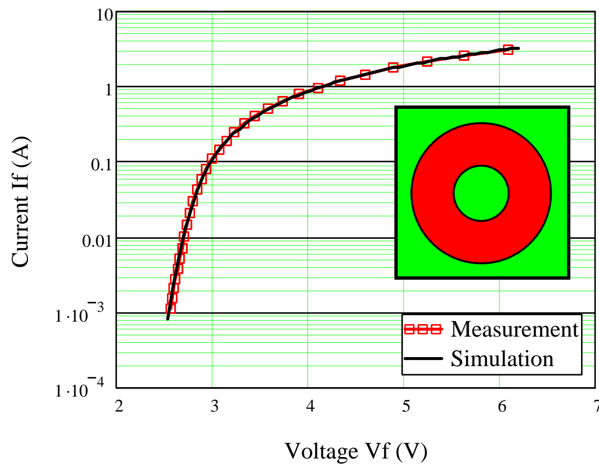
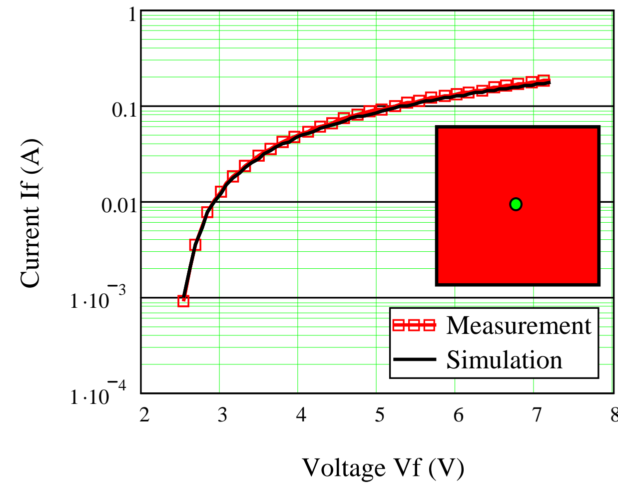
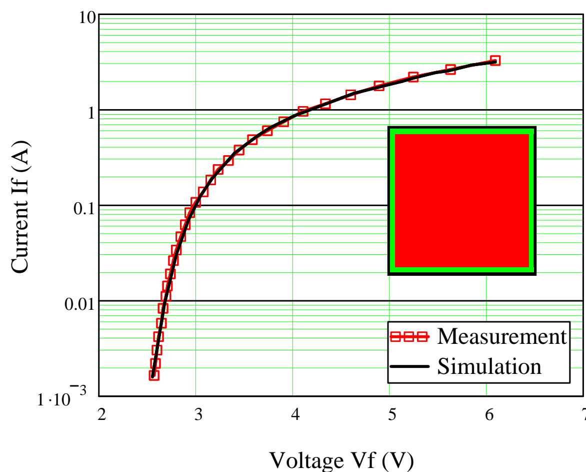
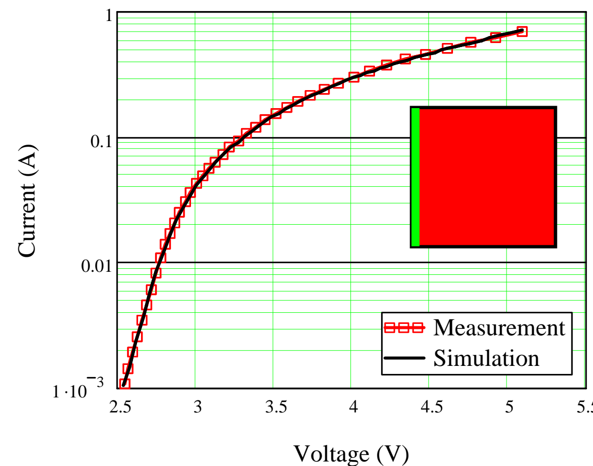
IV-Curves of Various Primary Emitter Layouts

- Simulations match up accurately measurement curves at constant 30°C junction temperature (pulse operation). Wafer near neighbor devices.









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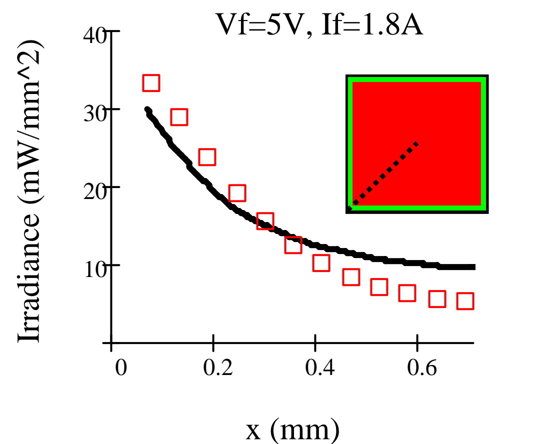
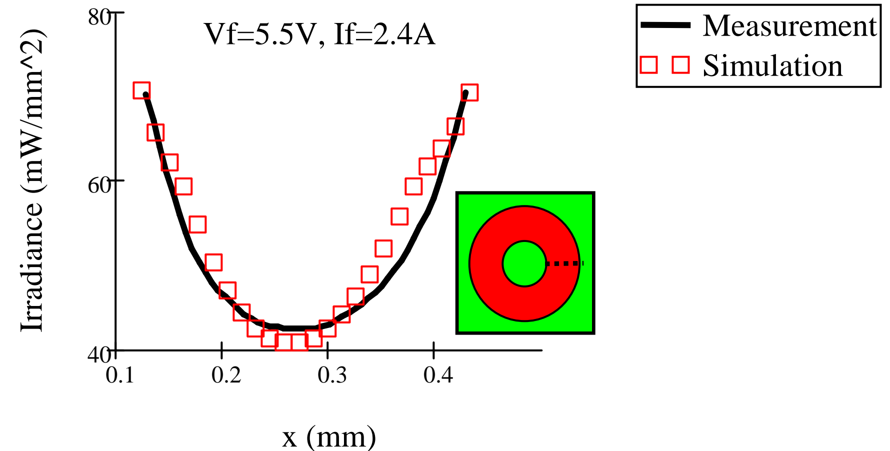
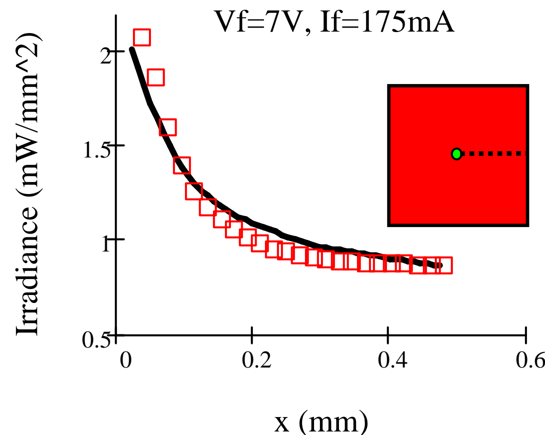
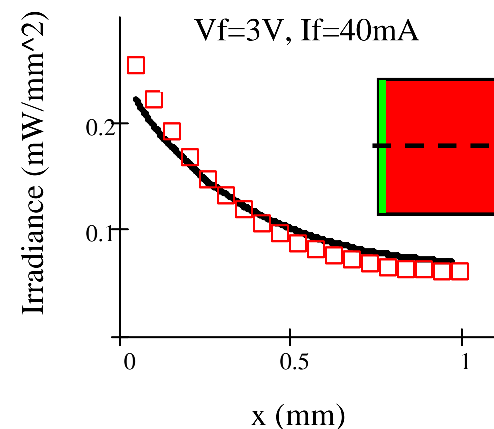
Surface Brightness of Various Primary Emitter Layouts

- Predictions within 15% error at constant 30°C junction temperature (pulse operation). Wafer near neighbor devices.









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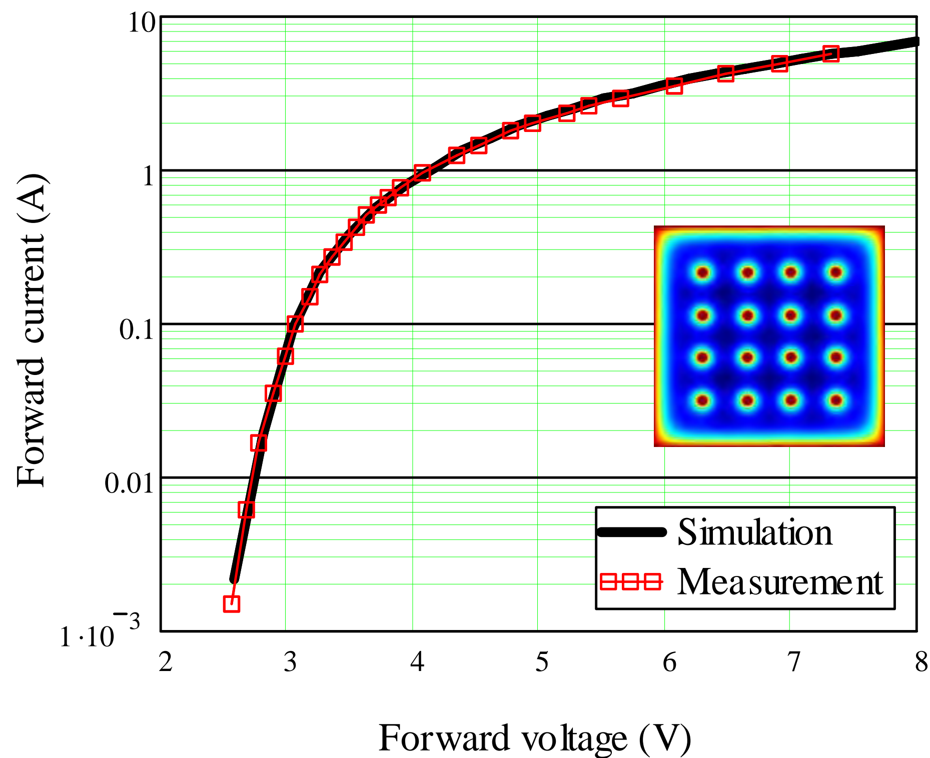
IV-Curves of a LUXEON® K2 Emitter without Self-Heating

- Experimental and simulated IV-curve characteristics at constant 90°C under pulse operation (i.e. without self-heating)



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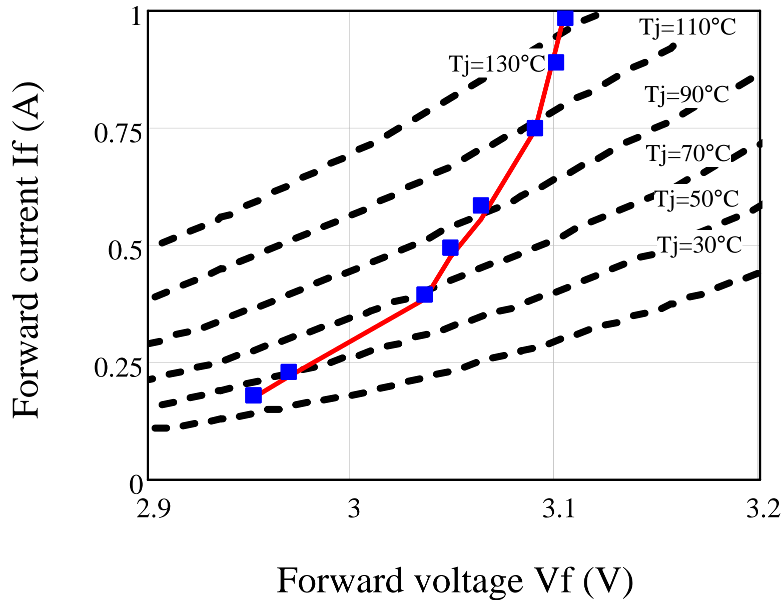
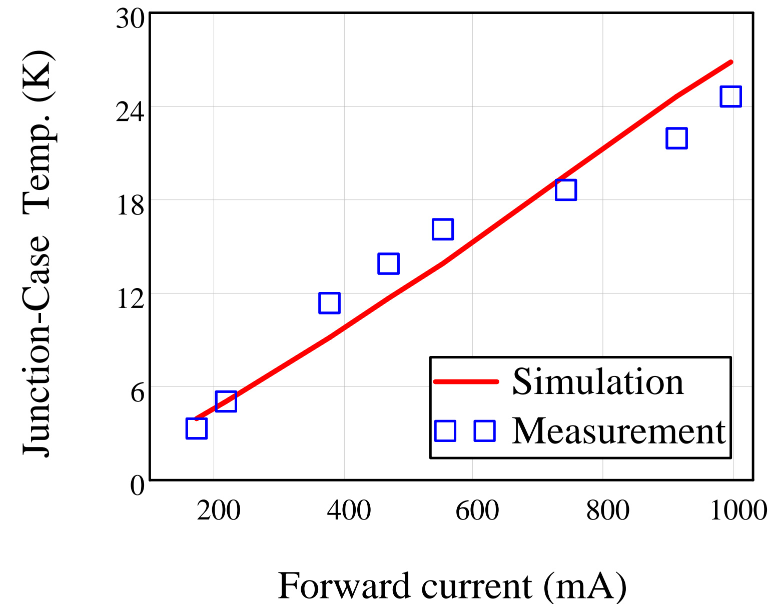
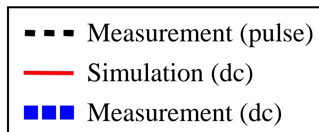
IV-Curves of a LUXEON® K2 Emitter with Self-Heating

- Experimental and simulated IV-curve characteristics under dc operation (i.e. with self-heating)







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Summary and Conclusions

- 3D FE model is shown to be an effective tool to analyse the electro-thermal behaviour of power LEDs
- Current crowding, forward voltage, self-heating, average thermal resistance and hot spots have been accurately modelled and validated over a wide range of operating conditions
- Simple model implementation based on a single subdomain and distributed resistance boundary conditions
- Four basic electric parameters to describe electrical behaviour are experimentally characterised and expressed in Comsol by means of LUTs
- Algorithm of system identification implemented in the Script language has been proposed for the extraction of the LED active region electrical characteristics from experimental data

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