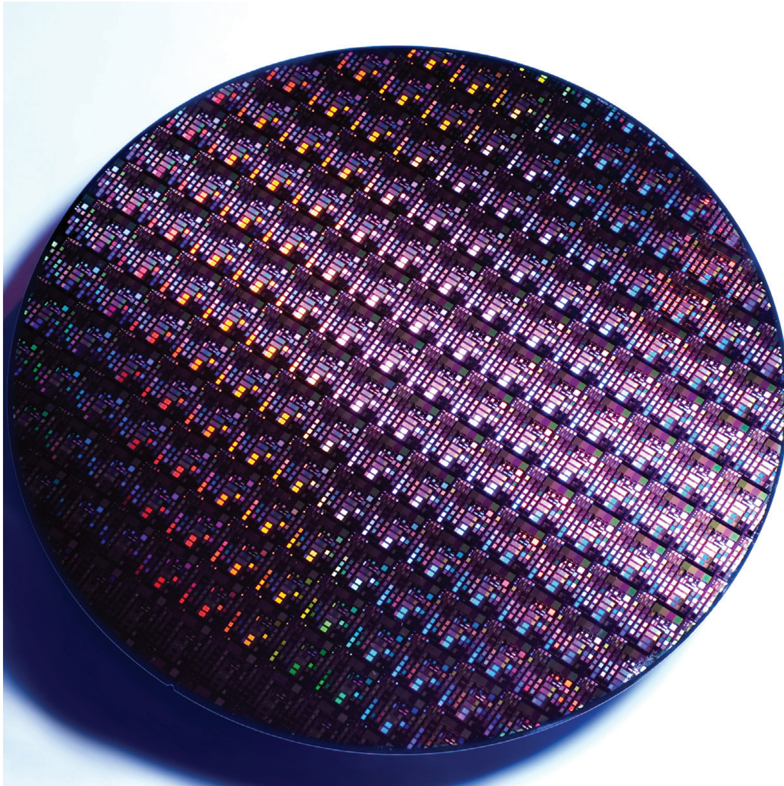

300mm semiconductor wafer patterned using multiple photolithography steps.

PUSHING THE LIMITS OF CHIP DENSITY

Researchers at Tokyo Electron in Austin, Texas, have created a finite element simulation to predict whether integrated circuit features will survive the manufacturing process

By **EDWARD BROWN**

MOORE'S LAW STATES that the number of transistors that can be economically placed on an integrated circuit doubles every two years. Although it's called a law, it's really a goal—a goal that chip manufacturers have successfully met since 1965. There are, however, serious technological challenges that must be solved in order to continue to achieve that goal.

Tokyo Electron America (TEL) produces manufacturing tools vital to the processing of integrated circuits that proactively support the industry's growth. TEL researchers Derek Bassett and Michael Carcasi are using COMSOL Multiphysics to economically build accurate solutions to ensure that these tools remain effective even as pattern features and spacings continue to shrink.

» THE PHOTOLITHOGRAPHY PROCESS

THE PROCESS USED for manufacturing integrated circuits is photolithography. A typical device can require as many as 200 cleaning and photolithography steps combined. Since patterning and cleaning is done throughout the process, a failure can be very costly. There can be more than 500 logic chips or more than 2,000 memory chips on each standard 300-millimeter wafer, and the wafers are produced at the rate of 100 to 200 wafers per hour. The failure of just a few wafers because of improper cleaning can cost millions of dollars in lost production.

» PATTERN COLLAPSE

PATTERN COLLAPSE IS a major concern in the development and cleaning processes. As the cleaning fluid evaporates from between two features, it exerts relatively large surface tension forces, which tend to make the features bend. Once the fluid has completely evaporated, the features may return to their normal shape, which is the desired result. But if the features are permanently deformed, the chip will be ruined (see Figure 1).

As the density of features per chip increases, cleaning and development problems become more difficult. Every few years, the minimum feature (or node) size is reduced — a tendency called node shrink. The distance between features also decreases, causing the increased surface tension forces to be able to bend the features (see Figure 2). Cleaning and development become more difficult,

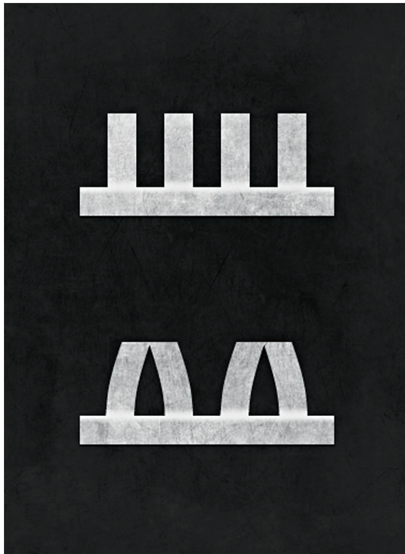

FIGURE 1: Pattern collapse: On top, features have returned to the unstressed position. Below, van der Waals forces dominate, features touch, and a defect that causes a chip failure is created.

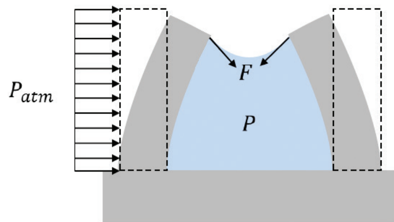

FIGURE 2: Surface tension: The cleaning fluid trapped between the features exerts forces on them capable of deforming their original shape. These forces originate from the Laplace pressure (Patm−P) and contact line forces (F).

so avoiding pattern collapse becomes more critical and more challenging.

Whether or not the pattern will collapse is a function of the aspect ratio, the ratio of height to thickness, and the stiffness of the feature materials as measured by their Young's modulus. The chemistry and physics dictate a minimum feature height below which the process will not be reliable; the feature width is constantly being reduced because of the need for increased density, however. The photoresist material for logic chips is prone to undergo pattern collapse because it is soft. The problems with memory chips are due to the increasing height and thinning width, which make it difficult to reach between the features for complete cleaning.

» WHY SIMULATION?

SINCE PATTERN COLLAPSE is sensitive to material and geometric parameters, it can become a resource-consuming task to understand which conditions give rise to it. Making wafers with all (or even many) of the possible features for experimental testing can mean months of process development and costs in the

FIGURE 3: Von Mises stress and deformation for two different features shapes.

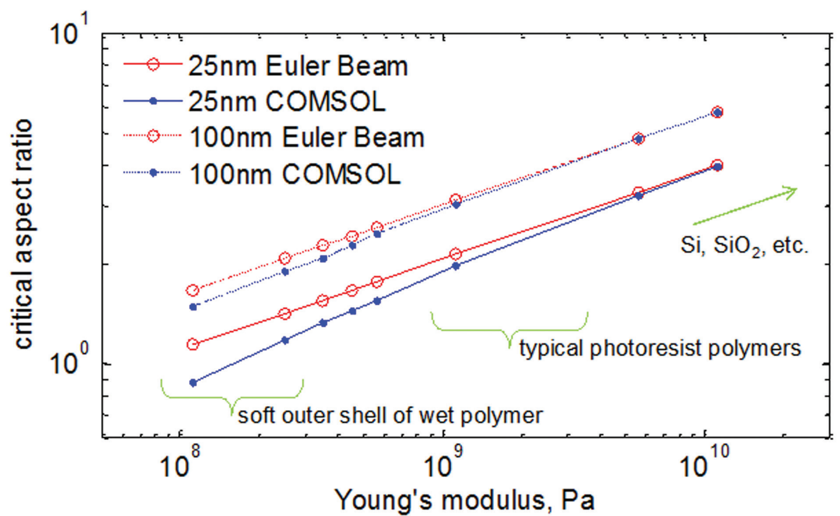

FIGURE 4: Comparison of the solutions using the 2-D finite element simulation and the 1-D Euler-Bernoulli equations. Finite element simulations should be used for lower aspect ratios.

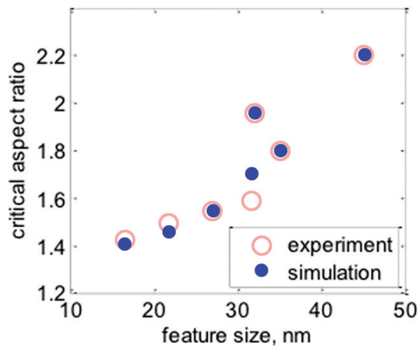

FIGURE 5: Simulation mimics experimental results correctly. [Yoshimoto, K., Higgins, C., Raghunathan, A., Hartley, J., Goldfarb, D., Kato, H., Petrillo, K., Colburn, M., Schefske, J., Wood, O., Wallow, T., "Revisit Pattern Collapse for 14nm Node and Beyond," Proc. SPIE 7972 (2011).]

Michael Carcasi, senior research scientist, and Derek Bassett, research scientist, of TEL.

millions of dollars. Simulations let researchers probe a wide parameter space relatively quickly and inexpensively. Occasionally, a small number of patterned wafers are made for physical testing, but those are used to verify the simulations once a large number of possibilities have been screened out. In other words, the scientists at TEL use simulation for greater focus in their research.

» SIMULATION ON THE NANOMETER LEVEL

SIMULATION HAS TRADITIONALLY been based on the Euler-Bernoulli beam equation, which generates a 1-D model. This has worked adequately in the past, but its accuracy begins to fail as aspect ratios shrink.

Derek Bassett, Michael Carcasi, and the team at TEL therefore chose to create a 2-D finite element model in COMSOL Multiphysics to solve the problem. Because the fluid evaporates much more slowly than the speed at which the features can bend, the system can be modeled as a series of steady-state calculations with the surface tension forces as boundary conditions. They developed techniques that enable solutions for a variety of geometries rather than just rectangles (see Figure 3). Their approach takes into account that at the molecular level, the interface between water and air doesn't go immediately from gas to liquid—there is a diffuse region of several nanometers in between. This provides a more realistic result for deformation along the contact line.

> *"Simulations let researchers probe a wide parameter space relatively quickly and inexpensively.*

Comparison of the solutions using the 2-D finite element model and the 1-D Euler-Bernoulli equations shows that predictions of pattern collapse match well for high-aspect-ratio structures made of stiff materials but diverge widely as the aspect ratio decreases (see Figure 4).

The 2-D simulation results were also compared with experimental data from the literature and were found to correctly predict the critical aspect ratio for collapse (see Figure 5).

» MOVING THE INDUSTRY FORWARD

COMSOL MULTIPHYSICS is an excellent means of dealing with the difficult problem of anticipating pattern collapse. Bassett and Carcasi feel it is by far the easiest finite element simulation software to use, saying that COMSOL makes it much easier to develop a model with custom mathematics and physics in order to test the results of proposed changes without the difficulty of writing and compiling code.

COMSOL Multiphysics has proven to be an important tool for evaluating solutions to the problems of higher pattern density. This will enable TEL to anticipate future trends so that it can quickly come up with solutions to move the industry forward. ◎